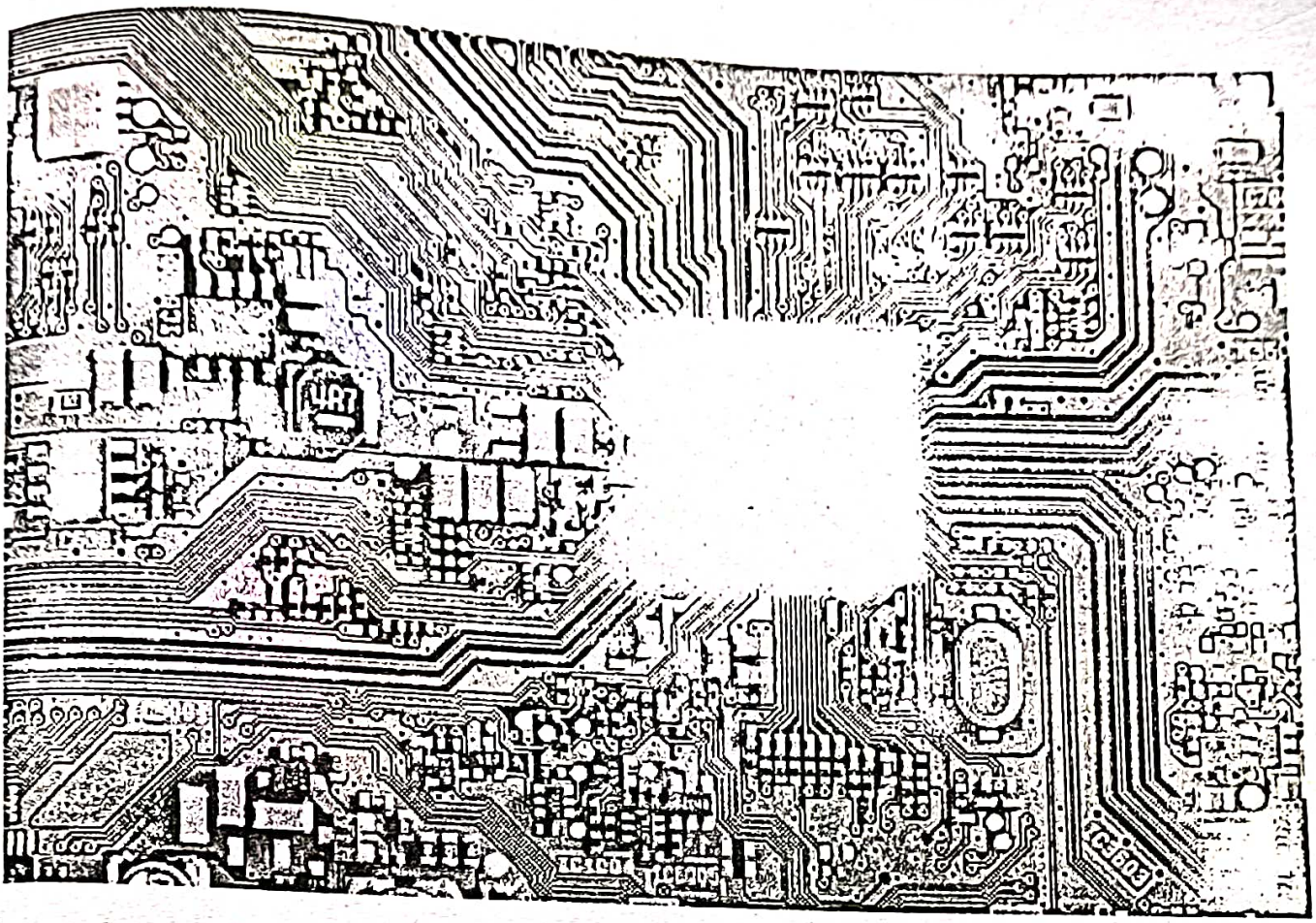


LINEAR INTEGRATED CIRCUITS

SYLLABUS

Chapter	Name of the Topic	
Unit I	**IC Fabrication and Circuit Configuration for Linear IC** Advantages of ICs over discrete components – Manufacturing process of monolithic Ics Construction of monolithic bipolar transistor – Monolithic diodes – Integrated Resistors Monolithic Capacitors – Inductors. Current mirror and current sources, Current sources as active loads, Voltage sources, Voltage References, BJT Differential amplifier with active loads, General operational amplifier stages and internal circuit diagrams of IC 741, DC and AC performance characteristics, slew rate, Open and closed loop Configurations.	14
Unit II	**Applications Of Operational Amplifiers** Sign Changer, Scale Changer, Phase Shift Circuits, Voltage Follower, V-to-I and I-to-V converters, adder, subtractor, Instrumentation amplifier, Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier, Comparators, Schmitt trigger, Precision rectifier, peak detector, clipper and clamper, Low-pass, high-pass and band pass Butterworth filters.	12
Unit III	**Analog Multiplier and PLL** Analog Multiplier using Emitter Coupled Transistor Pair -Gilbert Multiplier cell – Variable trans conductance technique, analog multiplier ICs and their applications, Operation of the basic PLL, Closed loop analysis, Voltage controlled oscillator, Monolithic PLL IC 565, application of PLL for AM detection, FM detection, FSK modulation and demodulation and Frequency synthesizing.	12
Unit IV	**Analog to digital and digital to analog converters** Analog and Digital Data Conversions, D/A converter –specifications - weighted resistor type, R-2R Ladder type, Voltage Mode and Current-Mode R2R Ladder types switches for D/A converters, high speed sample-and-hold circuits, A/D Converters specifications Flash type – Successive Approximation type Single Slope type – Dual Slope type - A/D Converter using Voltage- to-Time Conversion – Over sampling A/D Converters.	10
Unit V	**Waveform generators and special function ICs** Sine-wave generators, Multivibrators and Triangular wave generator, Saw-tooth wave generator, ICL8038 function generator, Timer IC 555, IC Voltage regulators – Three terminal fixed and adjustable voltage regulators - IC 723 general purpose regulator Monolithic switching regulator, Switched capacitor filter IC MF10, Frequency to Voltage and Voltage to Frequency converters, Audio Power amplifier, Video Amplifier, Isolation Amplifier, Opto- couplers and fibre optic IC.	12
	TOTAL	64

UNIT 01

IC FABRICATION AND CIRCUIT CONFIGURATION FOR LINEAR IC

QUESTIONS AND ANSWERS

Q1. Write the Advantage of ICs over the integrated circuits.

Ans. Advantages of IC integrated circuits

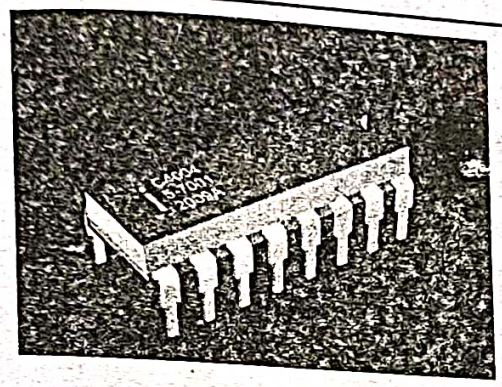


Fig. Integrated circuits

1. The entire physical size of IC is extremely small than that of discrete circuit.
2. The weight of an IC is very less as compared entire discrete circuits.
3. It's more reliable.
4. Because of their smaller size it has lower power consumption.
5. It can easily replace but it can hardly repair, in case of failure.
6. Because of an absence of parasitic and capacitance effect it has increased operating speed.

Q2. Describe the Manufacturing process of monolithic Ics.

Or, State the Construction of monolithic bipolar transistor.

Ans. Monolithic IC Manufacturing Process

For the manufacture and production of the monolithic IC, all circuit components and their interconnections are to be formed in a single thin wafer. The different processes carried out for achieving this are explained below.

1. **P-layer Substrate Manufacture :** Being the base layer of the IC, the P-type is silicon is first built for the IC. A silicon crystal of P-type is grown in dimensions of 250mm length and 25mm diameter. The silicon is then cut into thin slices with high precision using a diamond saw. Each wafer will precisely have a thickness of 200 micrometer and a diameter of 25 mm. These thin slices are termed wafers. These wafers may be circular or rectangular in shape with respect to the shape of the IC. After cutting hundreds of them each wafer is polished and cleaned to form a P-type substrate layer.
2. **N-type Epitaxial Growth :** The epitaxial groth process of a low resistive N-type over a high resistive P-type is to be carried out. This is done by placing the n-type layer on top of the P-type and heating then inside a diffusion furnace at very high temperature (nearly 120^0C). After heating, a gas mixture f Silicon atoms and pentavalent atoms are also passed over the layer. This forms the epitaxial layer on the substrate. All the components required for the circuit are built on top of this layer. The layer is then cooled down, polished and cleaned.
3. **The Silicon Dioxide Insulation Layer :** As explained above, this layer is required contamination of the N-layer epitaxy. This layer is only 1 micrometer thin and is grown by exposing the epitaxial layer to oxygen atmosphere at 1000C. A detailed image showing the P-type, N-type epitaxial layer and SiO_2 layer is given below.

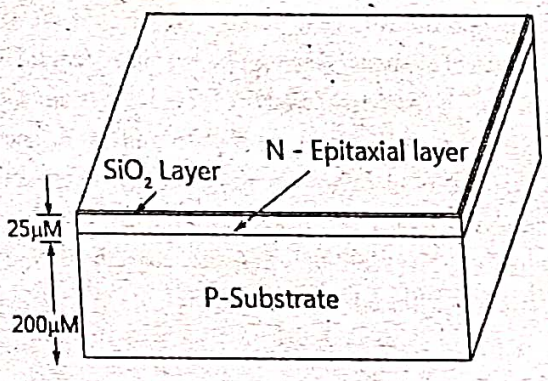


Fig. Monolithic IC-Substrates and Layers

4. **Photolithographic Process for SiO_2 :** To diffuse th impurities with the N-type epitaxial region, the silico

dioxide layer has to be etched in selected areas. Thus openings must be brought at these areas through photolithographic process. In this process, the SiO2 layer is coated with a thin layer of a photosensitive material called photoresist. A large black and white pattern is made in the desired patter, where the black pattern represents the area of opening and white represents the area that is left idle. This pattern is reduced in size and fit to the layer, above the photoresist. The whole layer is then exposed to ultraviolet light. Due to the exposure, the photoresist right below the white pattern becomes polymerized. The pattern is then removed and the wafer is developed using a chemical like trichloroethylene. The chemical dissolves the unpolymerized portion of the photoresist film and leaves the surface. The oxide not covered by polymerised photoresist is then removed by immersing the chip in an etching solution of HCl.

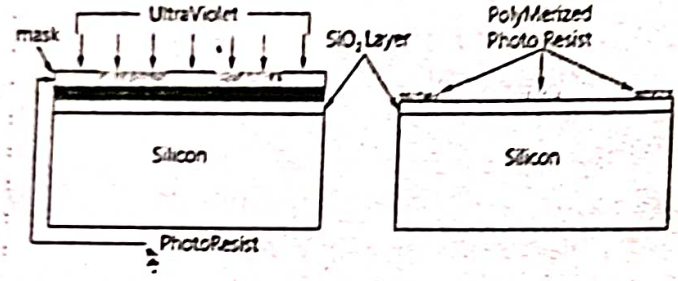


Fig. Monolithic IC - Photolithographic-Process

5. *Isolation Diffusion :* fter photolithographic process the remaining SiO_2 layer serves as a mask for the diffusion of acceptor impurities.. From the figure below you can see that the isolation islands look like back-to-back P-N junctions. The main use if this is to allow electrical isolation between the different components inside the IC. Each electrical element is later on formed in a separate isolation island. The bottom of the N-type isolation island ultimately forms the collector of an N-P-N transistor. The P-type substrate is always kept negative with respect to the isolation islands and provided with reverse bias at P-N junctions. The isolation will disappear if the P-N junctions are forward biased.

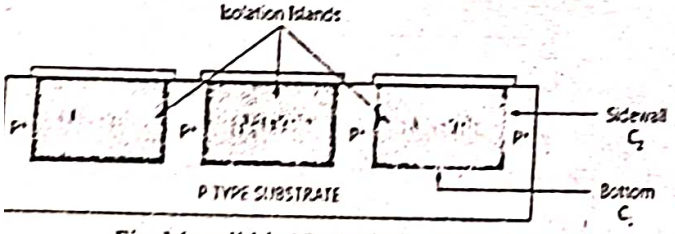


Fig. Monolithic IC - Isolation Diffusion

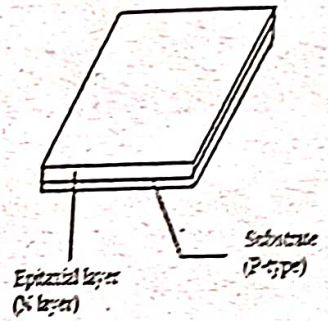
An effect of capacitance is produced in the region where the two adjoining isolation islands are connected to the type substrate. This is basically a parasitic capacitance that will affect the performance of the IC. This total capacitance is divided into two.

Construction of monolithic bipolar transistor :

The fabrication of a monolithic transistor includes the following steps.

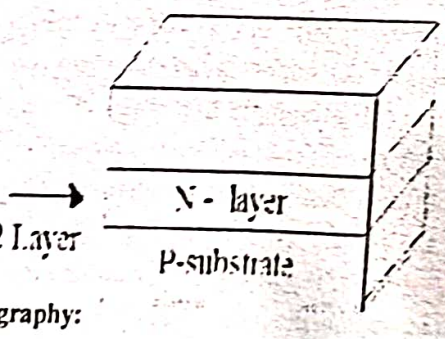
1. *Epitaxial growth*
2. *Oxidation*
3. *Photolithography*
4. *Isolation diffusion*
5. *Base diffusion*

1. **Epitaxial growth :** The first step in transistor fabrication is creation of the collector region. We normally require a low resistivity path for the collector current. This is due to the fact that, the collector contact is normally taken at the top, thus increasing the collector series resistance and the $V_{CE(Sat)}$ of the device.

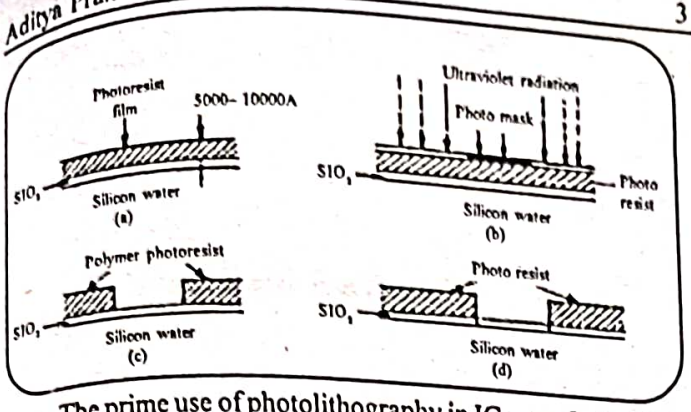


The higher collector resistance is reduced by a process called buried layer as shown in figure. In this arrangement, a heavily doped 'N' region is sandwiched between the N-type epitaxial layer and P –type substrate.The subsequent diffusions are done in this epitaxial layer. All active and passive components are formed on the thin N-layer epitaxial layer grown over the P-type substrate.

2. **Oxidation :** As shown in figure, a thin layer of silicon dioxide (SiO2) is grown over the N-type layer by exposing the silicon wafer to an oxygen atmosphere at about 10000 C.



3. **Photolithography:**



The prime use of photolithography in IC manufacturing is to selectively etch or remove the SiO_2 layer. As shown in figure, the surface of the oxide is first covered with a thin uniform layer of photosensitive emulsion (Photo resist). The mask, a black and white negative of the requied pattern, is placed over the structure. When exposed to ultraviolet light, the photo resist under the transparent region of the mask becomes poly-merized. The mask is then removed and the wafer is treated chemically that removes the unexposed portions of the photoresist film.

4. **Isolation Diffusion :** The integrated circuit contains many devices. Since a number of devices are to be fabricated on the same IC chip, it becomes necessary to provide good isolation between various components and their interconnections.

The most important techniques for isolation are:

1. PN junction Isolation
2. Dielectric Isolation

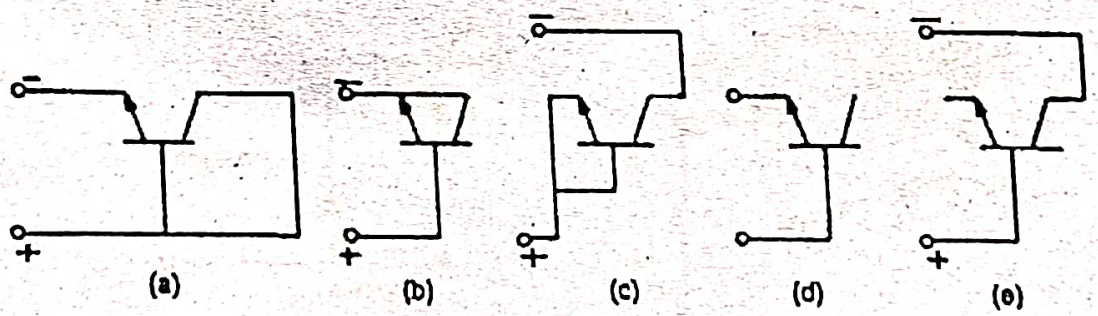
In PN junction isolation technique, the P+ type impurities are selectively diffused into the N-type epitaxial layer so that it touches the P-type substrate at the bottom. This method generated N-type isolation regions surrounded by P-type moats.

5 **Base diffusion :** Formation of the base is a critical step in the construction of a bipolar transistor. The base must be aligned, so that, during diffusion, it does not come into contact with either the isolation region or the buried layer. Frequently, the base diffusion step is also used in parallel to fabricate diffused resistors for the circuit.

Q3. Describe Monolithic diodes.

Ans. The diode used in integrated circuits are made using transistor structures in one of the five possible connections. The three most popular structures are shown in figure. The diode is obtained from a transistor structure using one of the following structures.

Characteristic	(a) $V_{CB} = 0$	(b) $V_{CE} = 0$	(c) $V_{EB} = 0$	(d) $I_C = 0$	(e) $I_E = 0$
Breakdown voltage in volts	7	7	55	7	55
Storage time, n sec	9	100	53	56	85
Forward voltage in volts	.85	.92	.94	.96	.95



1. The emitter-base diode, with collector short circuited to the base.
2. The emitter-base diode with the collector open and
3. The collector–base diode, with the emitter open-circuited.

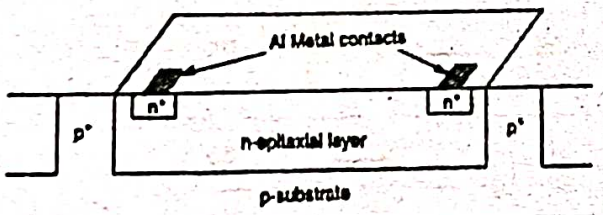
The choice of the diode structure depends on the performance and application desired. Collector-base diodes have higher collector-base arrays breaking rating, and they are suitable for common-cathode diode arrays diffused within a single isolation island. The emitter-base diffusion is very popular for the fabrication of diodes, provided the reverse-voltage requirement of the circuit does not exceed the lower base-emitter breakdown voltage.

Q4. Explain the Integrated Resistors and its types.

Ans. Integrated Resistors: A resistor in a monolithic integrated circuit is obtained by utilizing the bulk resistivity of the diffused volume of semiconductor region. The commonly used methods for fabricating integrated resistors are :

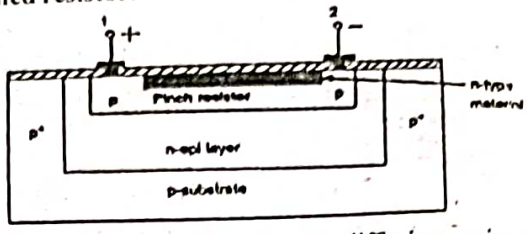
1. Diffused
2. Epitaxial
3. Pinched
4. Thin film techniques.

1. **Diffused Resistor:** The diffused resistor is formed in any one of the isolated regions of epitaxial layer during base or emitter diffusion processes. This type of resistor fabrication is very economical as it runs in parallel to the bipolar transistor fabrication. The N-type emitter diffusion and P-type base diffusion are commonly used to realize the monolithic resistor.
2. **Epitaxial Resistor:**



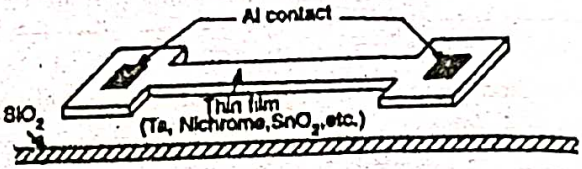
The N-epitaxial layer can be used for realizing large resistance values. The figure shows the cross-sectional view of the epitaxial resistor formed in the epitaxial layer between the two N+aluminium metal contacts.

3. **Pinched resistor:**



The sheet resistance offered by the diffusion regions can be increased by narrowing down its cross-sectional area. This type of resistance is normally achieved in the base region. Figure shows a pinched base diffused resistor. It can offer resistance of the order of mega ohms in a comparatively smaller area. In the structure shown, no current can flow in the N-type material

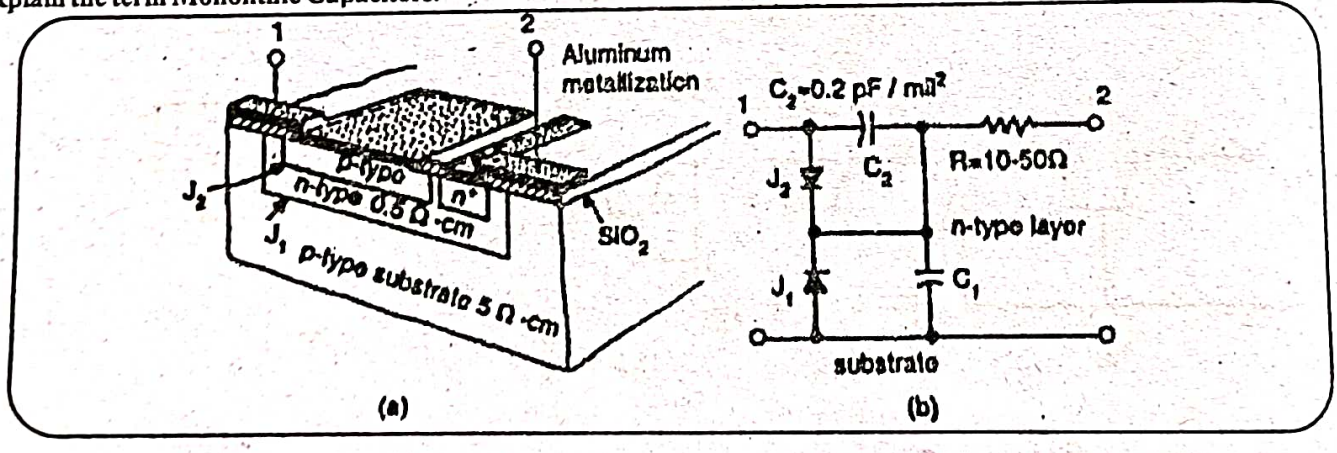
4. **Thin film resistor :**



The thin film deposition technique can also be used for the fabrication of monolithic resistors. A very thin metallic film of thickness less than 1μm is deposited on the silicon dioxide layer by vapour deposition techniques. Normally, Nichrome (NiCr) is used for this process.

Q5. Explain the term Monolithic Capacitors.

Ans.



Monolithic capacitors are not frequently used in integrated circuits since they are limited in the range of values obtained and their performance. There are, however, two types available, the junction capacitor is a reverse biased PN junction formed by the collector-base or emitter-base diffusion of the transistor. The capacitance is proportional to the area of the junction and inversely proportional to the depletion thickness.

$C \propto A$, where a is the area of the junction and

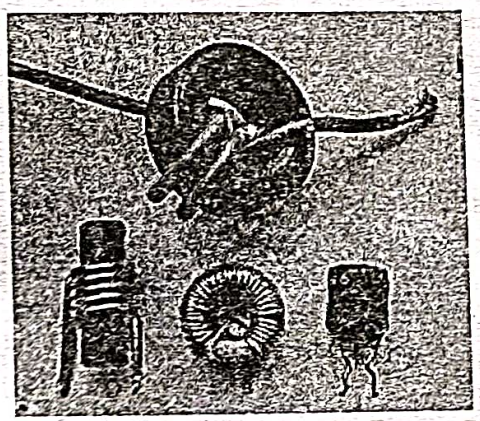
$C \propto T$, where t is the thickness of the depletion layer.

The capacitance value thus obtainable can be around 1.2nF/mm2

The thin film or metal oxide silicon capacitor uses a thin layer of silicon dioxide as the dielectric. One plate is the connecting metal and the other is a heavily doped layer of silicon, which is formed during the emitter diffusion. This capacitor has a lower leakage current and is non-directional, since emitter plate can be biased positively. The capacitance value of this method can be varied between 0.3 and 0.8nF/mm2.

Q6. Define Inductor.

Ans. An inductor, also called a coil, choke, or reactor, is a passive two-terminal electrical component that stores energy in a magnetic field when electric current flows through it. An inductor typically consists of an insulated wire wound into a coil.



When the current flowing through the coil changes, the time-varying magnetic field induces an electromotive force (e.m.f.) (voltage) in the conductor, described by Faraday's law of induction. According to Lenz's law, the induced voltage has a polarity (direction) which opposes the change in current that created it. As a result, inductors oppose any changes in current through them. An inductor is characterized by its inductance, which is the ratio of the voltage to the rate of change of current.

Q7. Describe Current mirror and current sources explain with ckt diagram.

Ans.1. Current mirror : The circuit is used to copy the flow of current in one active device and controlling the flow of current in another device by maintaining the output current stable instead of loading is known as a current mirror. Theoretically, a perfect current mirror is an inverting current amplifier. The main function of this amplifier is to reverse the direction of the flow of current. The main function of the current mirror is to provide active loads as well as bias currents to circuits and also used to form a more practical current source.

Current Mirror Circuit :

Generally, the designing of current mirror circuits can be done with two main transistors and even though other devices like FETs also used. Some of these circuits may utilize the above two transistors for allowing the performance level to be enhanced. As the name suggests, it copies the flow of current in one active device whereas, in another active device, it maintains the output current stable instead of loading. The copied current is a constant current.

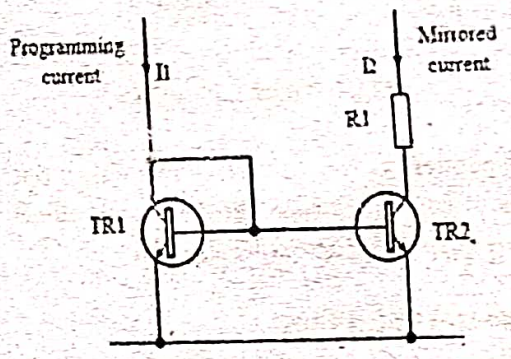


Fig. Current Mirror Circuit

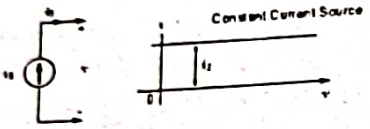
The current mirror circuit diagram is shown below. This circuit can be built with two transistors, where one of the transistors base and collector terminals are connected whereas in other it doesn't. In the circuit, both the transistor's base terminals are connected whereas the emitter terminals are given to GND. In this circuit, both the transistors work similarly.

Q8. Describe the term current sources also write their types and explain them with ckt diagram.

Ans. Current sources : In an electrical network, current source and voltage source are the basic concepts behind many electrical applications. Let see the different types of current source...

1. **Ideal current source :** A current source which supplies the constant current to connected across the load circuit regardless of the voltage developed across its terminals. The loads may be resistive load or inductive load or capacitive load etc. The current source's internal resistance should be infinity. But in practice, we cannot construct ideal current source.

Ideal Current Sources



Ideal Current Sources vs Practical Current Sources

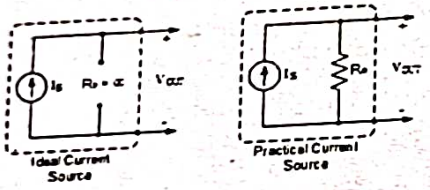
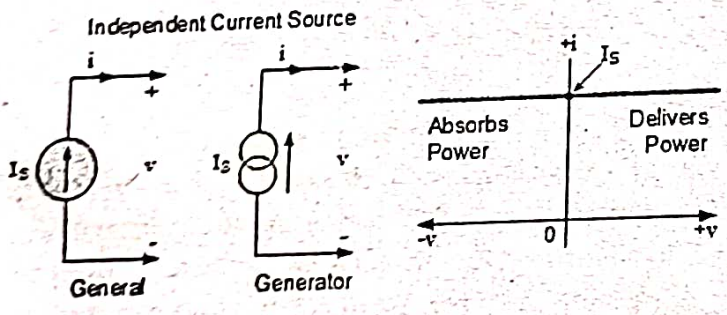
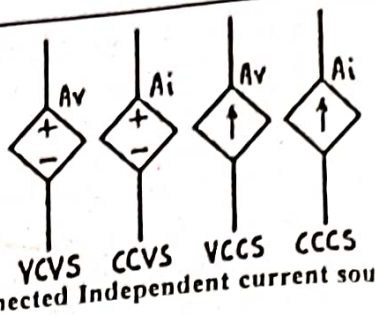


Fig. Ideal current source:

2. **Independent current source :** Supplies constant current to the circuit regardless of the load and the direction of the voltage appearing across its terminal.



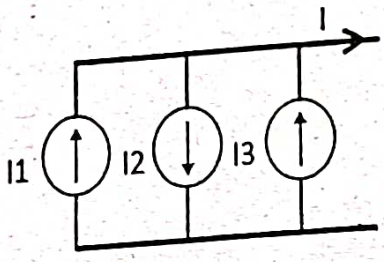
Symbolic representation:



3. **Series connected Independent current source:** To get output...
   1. All the current source should be in the same rating
   2. Polarity should be taken care of. The wrong polarity leads to reduced output.

Parallel connected Independent current source:

Parallel connected Independent current source



The parallel connected current sources is equivalent to the algebraic sum of single current sources.

$$I = I_1 - I_2 + I_3$$

4. **Dependent current sources :** In this, the current source is depending upon a circuit's existing current or voltage sources (the source will be placed in the same circuit, some other location)
   1. Voltage controlled Current source.
   2. Current controlled current source.
5. **Voltage controlled Current source :** The source delivers the current (flow of electron) as per the voltage of the dependent element in the same network

Example:

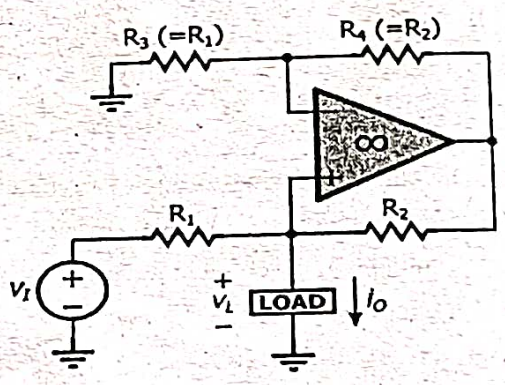


Fig. Voltage controlled Current source

6. **Current Controlled current source :** The source delivers current as per the current of the dependent element in the circuit.

Example:

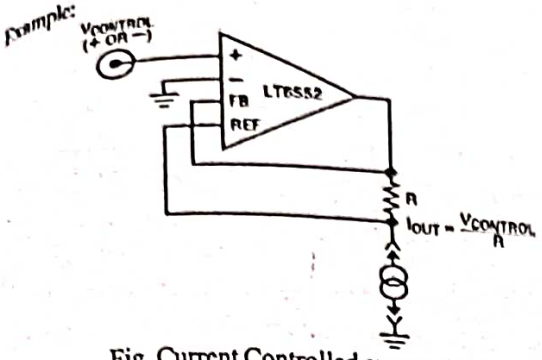


Fig. Current Controlled current Source

Q9. Write short notes about Current sources as Active loads.

Ans. The current source can be used as an active load in both analog and digital IC's.The current source can be used as an active load in both analog and digital IC's. The active load realized using current source in place of the passive load (i.e. a resistor) in the collector arm of differential amplifier makes it possible to achieve high voltage gain without requiring large power supply voltage. The active load so achieved is basically R0 of a PNP transistor.

Q10. Describe Voltage sources and draw the suitable ckt diagram for the same.

Ans. Voltage Sources : A voltage source is a circuit that produces an output voltage V0, which is independent of the load driven by the voltage source, or the output current supplied to the load. The voltage source is the circuit dual of the constant current source. A number of IC applications require a voltage reference point with very low ac impedance and a stable dc voltage that is not affected by power supply and temperature variations. There are two methods which can be used to produce a voltage source, namely,

1. Using the impedance transforming properties of the transistor, which in turn determines the current gain of the transistor and
2. Using an amplifier with negative feedback.

Voltage source circuit using Impedance transformation: The voltage source circuit using the impedance transforming property of the transistor is shown in figure. The source voltage Vs drives the base of the transistor through a series resistance RS and the output is taken across the emitter. From the circuit, the output ac resistance looking into emitter is given by

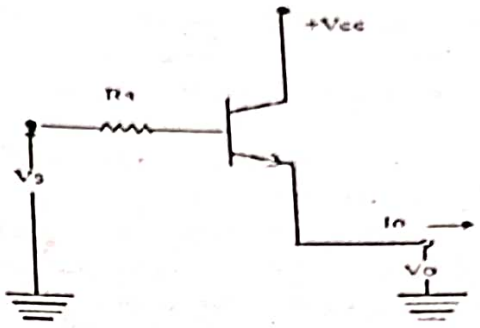


Fig. Voltage source circuit using Impedance transformation

$$\frac{d_0}{dI_0} = R_0 = \frac{R_s}{\beta+1} = r_{eb};$$

$$\because \beta >> 100, \quad R_0 = \frac{R_s}{\beta+1}$$

It is to be noted that, equation is applicable only for small changes in the output current. The load regulation parameter indicates the changes in V_0 resulting from large changes in output current I_0, Reduction in V_0 occurs as I_0 goes from no-load current to full-load current and this factor determines the output impedance of the voltage sources.

Q11. Describe Voltage References.

Ans. The circuit that is primarily designed for providing a constant voltage independent of changes in temperature is called a voltage reference. The most important characteristic of a voltage reference is the temperature coefficient of the output= reference voltage TcR , and it is expressed as .

$$T_{CR} = \frac{dV_R}{dT}$$

The desirable properties of a voltage reference are:

1. Reference voltage must be independent of any temperature change.
2. Reference voltage must have good power supply rejection which is as independent of the supply voltage as possible and
3. Output voltage must be as independent of the loading of

output current as possible, or in other words, the circuit should have low output impedance.

The voltage reference circuit is used to bias the voltage source circuit, and the combination can be called as the voltage regulator. The basic design strategy is producing a zero TCR at a given temperature, and thereby achieving good thermal ability. Temperature stability of the order of 100ppm/0 C is typically expected.

Voltage Reference circuit using temperature compensation scheme : The voltage reference circuit using basic temperature compensation scheme is shown below. This design utilizes the close thermal coupling achievable among the monolithic components and this technique compensates the known thermal drifts by introducing an opposing and compensating drift source of equal magnitude.

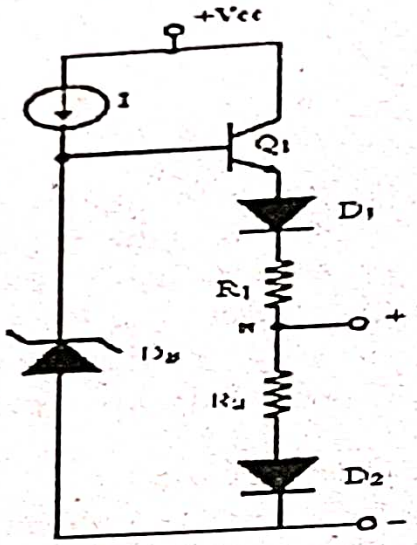


Fig. Voltage Reference circuit using temperature compensation scheme

A constant current I is supplied to the avalanche diode DB and it provides a bias voltage of VB to the base of Q_1. The temperature dependence of the VBE drop across Q_1 and those across D_1 and D_2 results in respective temperature coefficients. Hence, with the use of resistors R_1 and R_2 with tapping across them at point N compensates for the temperature drifts in the base-emitter loop of Q_1.

Q12. Explain BJT Differential Amplifier using active loads.

Ans. A simple active load circuit for a differential amplifier is the current mirror active load as shown in figure. The active load comprises of transistors Q_3 and Q_4 with the transistor Q_3 connected as a Diode with its base and collector shorted. The circuit is shown to drive a load RL. When an ac input voltage is applied to the differential amplifier, the various currents of the circuit are given by $IC4 = IC3 = IC1 = gmVid/2$ where $IC4 = IC3$ due to current mirror action.

$IC2 = -gmVid/2$.

We know that the load current IL entering the next stage is $IL = IC2 - IC4 = -gmVid/2 - gmVid/2 = -gmVid$

Then, the output voltage from the differential amplifier is given by $V0 = -ILRL = gm\,RLVid$. The ac voltage gain of the circuit is given by $Av = v0/vid = gmRL$. The amplifier can amplify the differential input signals and it provides single-ended output with a ground reference since the load RL is connected to only one output terminal. This is made possible by the use of the current mirror active load. The output resistance R_0 of the circuit is that offered by the parallel combination of transistors Q_2 (NPN) and Q_4 (PNP). It is given by $Rr = r02 \parallel r04$.

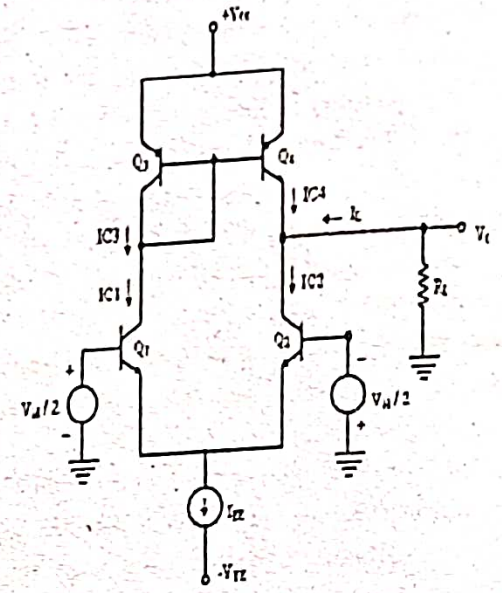


Fig. BJT Differential Amplifier using active loads.

Q13. Describe General Operational Amplifier stages and internal circuit diagrams of IC 741.

Ans. An operational amplifier generally consists of three stages, namely :

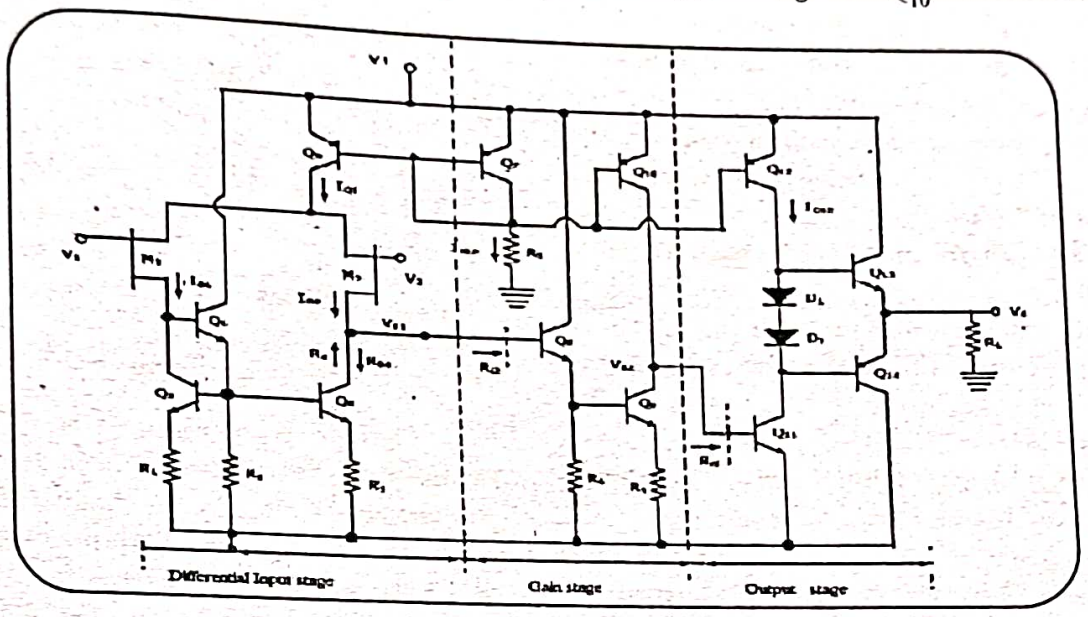
1. A differential amplifier
2. Additional amplifier stages to provide the required voltage gain and dc level shifting.
3. An emitter-follower or source follower output stage to provide current gain and low output resistance.

A low-frequency or dc gain of approximately 104 is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp. The

output voltage is required to be at ground, when the differential input voltages are zero, and this necessitates the use of dual polarity supply voltage. Since the output resistance of op-amp is required to be low, a complementary push-pull emitter – follower or source follower output stage is employed. Moreover, as the input bias currents are to be very small of the order of pico amperes, an FET input stage is normally preferred.

Input stage: The input differential amplifier stage uses p-channel JFETs M_1 and M_2. It employs a three-transistor active load formed by Q_3, Q_4, and Q_5. The bias current for the stage is provided by a two-transistor current source using PNP transistors Q_6 and Q_7. Resistor R_1 increases the o utput resistance seen looking into the collector of Q_4 as indicated by R04. This is necessary to provide bias current stability against the transistor parameter variations. Resistor R_2 establishes a definite bias current through Q_5.

Gain stage: The second stage or the gain stage uses Darlington transistor pair formed by Q_8 and Q_9 as shown in figure. The transistor Q_8 is connected as an emitter follower, providing large input resistance.Therefore, it minimizes the loading effect on the input differential amplifier stage. The transistor Q_9 provides an additional gain and Q_{10} acts as an active load for this stage.



Output stage: The final stage of the op-amp is a class AB complementary push-pull output stage. Q_{11} is an emitter follower, providing a large input resistance for minimizing the loading effects on the gain stage. Bias current for Q_{11} is provided by the current mirror formed by Q_7 and Q_{12}, through Q_{13} and Q_{14} for minimizing the cross over distortion. Transistors can also be used in place of the two diodes.

IC 741 Bipolar operational amplifier: The IC 741 produced since 1966 by several manufactures is a widely used general purpose operational amplifier. Figure shows that equivalent circuit of the 741 op-amp, divided into various individual stages. The op-amp circuit consists of three stages.

1. The input differential amplifier
2. The gain stage
3. The output stage.

A bias circuit is used to establish the bias current for whole of the circuit in the IC. The op-amp is supplied with positive and negative supply voltages of value ± 15V and the supply voltages as low as ±5V can also be used.

Bias Circuit:

The reference bias current IREF for the 741 circuit is established by the bias circuit consisting of two diodes-connected transistors Q_{11} and Q_{12} and resistor R5. The Widlar current source formed by Q_{11}, Q_{10} and R4 provide bias current for the differential amplifier stage at the collector of Q_{10}. Transistors Q_8 and Q_9 form another current mirror providing bias current for the differential amplifier.

Input stage: The input differential amplifier stage consists of transistors Q_1 through Q_7 with biasing provided by Q_8

through Q_{12}. The transistor Q_1 and Q_2 form emitter – followers contributing to high differential input resistance, and whose output currents are inputs to the common base amplifier using Q_3 and Q_4 which offers a large voltage gain. The transistors Q_5, Q_6 and Q_7 along with resistors R1, R2 and R3 from the active load for input stage. The single-ended output is available at the collector of Q_6. The two null terminals in the input stage facilitate the null adjustment.

Gain Stage: The Second or the gain stage consists of transistors Q_{16} and Q_{17}, with Q_{16} acting as an emitter – follower for achieving high input resistance. The transistor Q_{17} operates in common emitter configuration with its collector voltage applied as input to the output stage.

Output stage: The output stage is a class AB circuit consisting of complementary emitter follower transistor pair Q_{14} and Q_{20}. Hence, they provide an effective loss output resistance and current gain.

Q14. Describe AC and DC characteristics of Oprerational Amplifier.

Ans. For small signal sinusoidal (AC) application one has to know the ac characteristics such as frequency response and slew-rate.

AC characteristics :

1. Frequency Response: The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response. Op-amp should have an infinite bandwidth BW =8 (i.e.) if its open loop gain in 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency. But op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain after a certain frequency reached.

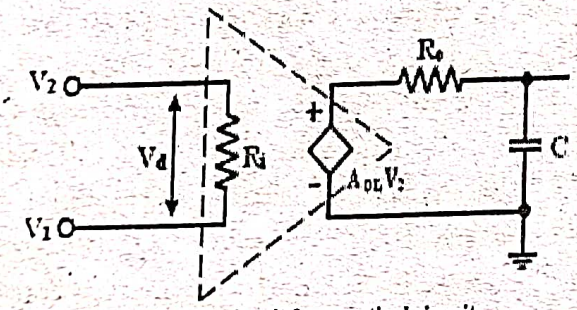


Fig. Equivalent circuit for practical circuit

There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C. Below fig is a modified variation of the low frequency model with capacitor C at the output.

There is one pole due to R0C and one -20dB/decade. The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig. f1 is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase angle of the open loop volt gain are f1 of frequency can be written as, The magnitude and phase angle characteristics:

1. For frequency f<< f1 the magnitude of the gain is 20 log AOL in db.
2. At frequency f = f1 the gain in 3 dB down from the dc value of AOL in db. This frequency fI is called corner frequency.
3. For f>> f1 the fain roll-off at the rate off -20dB/decade or. 6dB/decade.

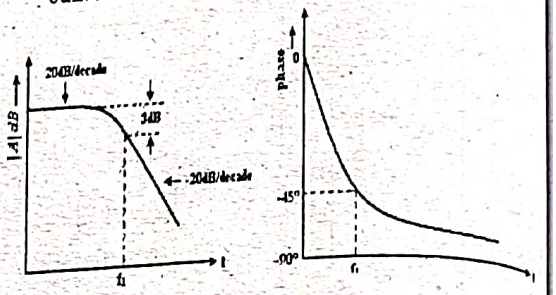


Fig. Frequency responce of op amp

From the phase characteristics that the phase angle is zero at frequency f = 0. At the corner frequency f1 the phase angle is /–45° (lagging and an infinite frequency the phase angle is –90 . It shows that a maximum of 90 phase change can occur in an op-amp with a single capacitor C. Zero frequency is taken as the decade below the corner frequency and infinite frequency is one decade above the corner frequency.

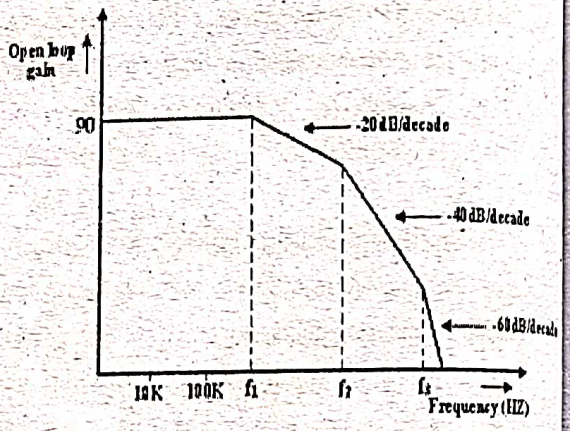


Fig. Roll off rate of OP amp gain

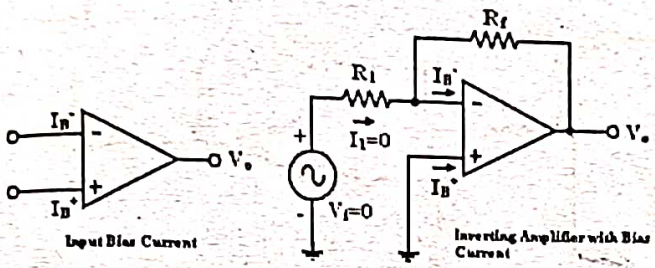
DC Characteristics of op-amp: Current is taken from the

source into the op-amp inputs respond differently to current andvoltage due to mismatch in transistor. DC output voltages are,

Input bias current Input offset current
Input offset voltage Thermal drift

1. **Input bias current :** The op-amp's input is differential amplifier, which may be made of BJT or FET.

In an ideal op-amp, we assumed that no current is drawn from the input terminals the base currents entering into the inverting and non-inverting terminals (IB- & IB+ respectively).Even though both the transistors are identical, IB- and IB+ are not exactly equal due to internal imbalance between the two inputs. Manufacturers specify the input bias current I_B



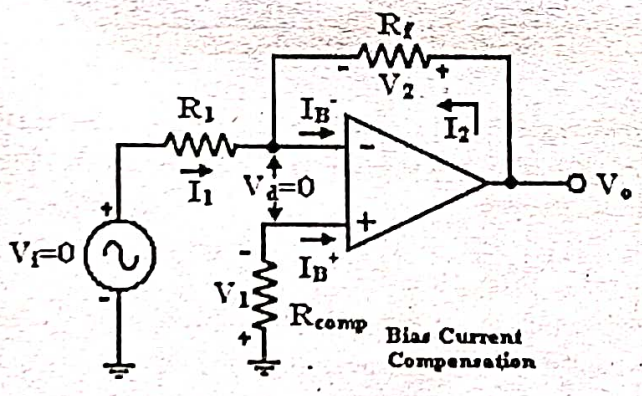
$$I_b = \frac{I_B^- + I_B^-}{2}$$

If input voltage Vi = 0V. The output Voltage Vo should also be (Vo = 0) but for IB = 500nA We find that the output voltage is offset by Op-amp with a 1M feedback resistor

$$Vo = 500nA X\ 1M = 500mV$$

The output is driven to 500mV with zero input, because of the bias currents.

In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated by a compensation resistor Rcomp has been added between the non-inverting input terminal and ground as shown in the figure below.



Current IB+ flowing through the compensating resistor Rcomp, then by KVL we get,

$I \quad _1 + 0 + V2 - Vo = 0$ (or)

$$Vo = V2 - V_1 \quad \text{--------(1)}$$

By selecting proper value of Rcomp, V2 can be cancelled with V_1 and the Vo = 0. The value of Rcomp is derived as

$V_1 = IB{+}Rcomp$ (or)

$$IB+ = V_1 / Rcomp \quad \text{————(2)}$$

The node 'a' is at voltage $(-V_1)$. Because the voltage at the non-inverting input terminal is $(-V_1)$. So with Vi = 0 we get,

$$I_1 = V_1 / R_1 \quad \text{————(3)}$$

$$I_2 = V_2 / Rf \quad \text{————(4)}$$

For compensation, Vo should equal to zero (Vo = 0, Vi = 0). i.e. from equation (3) $V_2 = V_1$. So that,

$$I_2 = V_1 / Rf \longrightarrow (5)$$

KCL at node 'a' gives,

$$IB- = I_2 + I_1 = (V_1/Rf) + (V_1/R_1)$$

$$= V_1(R_1 + Rf)/R_1Rf \quad \text{————(5)}$$

Assume IB – = IB+ and using equation (2) & (5) we get

$$V_1 (R_1 + R_f) / R_1R_f = V_1 / R_{comp}$$

$$R_{comp} = R_1 \| Rf \quad \text{————(6)}$$

i.e. to compensate for bias current, the compensating resistor, Rcomp should be equal to the parallel combination of resistor R_1 and Rf.

Input offset current:

- Bias current compensation will work if both bias currents IB+ and IB- are equal.
- Since the input transistor cannot be made identical. There will always be some small difference between IB+ and IB-. This difference is called the offset current

$$|Ios| = IB + - IB \quad \text{————(7)}$$

Offset current Ios for BJT op-amp is 200nA and for FET op-amp is 10pA. Even with bias current compensation, offset current will produce an output voltage when Vi = 0.

$$V_1 = I_B + R_{comp} \quad \text{.....(8)}$$

And $I_1 = V_1/R_1$ .....(9)

KCL at node a gives,

$$I_2 = (I_B^- - I_1) = I_B^- - \left(I_B^+ \frac{R_{comp}}{R_1} \right)$$

Again $V_0 = I2\ Rf - V_1$

$V_0 = I2\ Rf - IB{+}Rcomp$

$V_0 = 1M\,O \times 200nA$

$V_0 = 200mV$ with Vi = 0

Eq. (9) the offset current can be minimized by keeping

feedback resistance small.

- Unfortunately to obtain high input impedance, R1 must be kept large.
- R_1 large, the feedback resistor Rf must also be high. So as to obtain reasonable gain.

The T-feedback network is a good solution. This will allow large feedback resistance, while keeping the resistance to ground low (in dotted line).

- The T-network provides a feedback signal as if the network were a single feedback resistor.

By T to $\prod$ conversion,

$$R_f = \frac{R_t^2 + 2R_tR_s}{R_s}$$

To design T- network first pick Rt << Rf / 2 and=calculate

$$R_s = \frac{R_t^2}{R_f - 2R_t}$$

Input offset voltage:

In spite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminal to make output (Vo) = 0. This voltage is called input offset voltage Vos. This is the voltage required to be applied at the input for making output voltage to zero (Vo = 0).

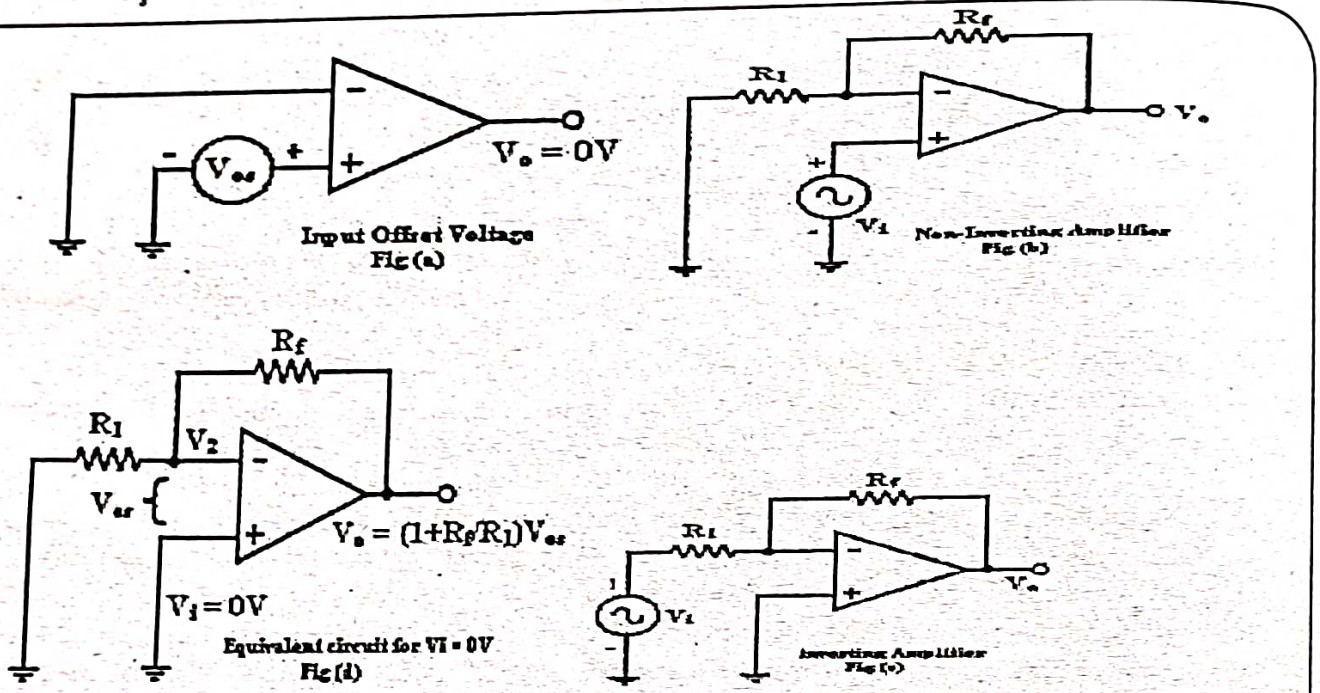


Fig.

Let us determine the Vos on the output of inverting and non-inverting amplifier. If Vi = 0 (Fig (b) and (c)) become the same as in figure (d).

Thermal drift: Bias current, offset current, and offset voltage change with temperature. A circuit carefully nulled at 25°C may not remain. So when the temperature rises to 35°C. This is called drift. Offset current drift is expressed in nA/°C. These indicate the change in offset for each degree Celsius change in temperature.

Q15. Describe Slew Rate and its reasons..

Ans. Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/μs.

Reason for Slew rate: There is usually a capacitor within 0, outside an op-amp oscillation. It is this capacitor which prevents the o/p voltage from fast changing input. The rate at which the volt across the capacitor increases is given by

feedback resistance small.

- Unfortunately to obtain high input impedance, R1 must be kept large.
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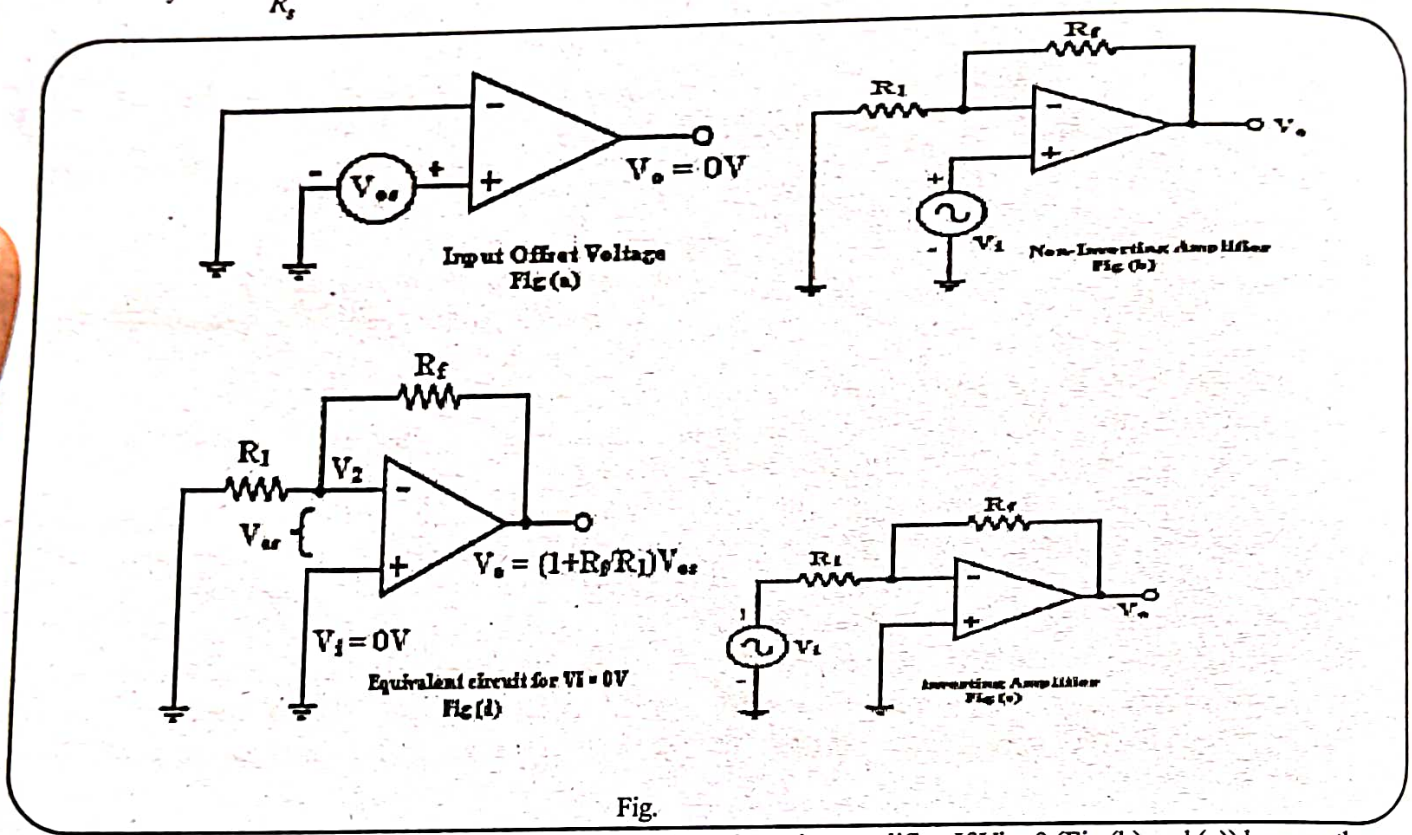

Fig.

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dVc/dt = I/C ------(1)

I -> Maximum amount furnished by the op-amp to capacitor C. Op-amp should have the either a higher current or small compensating capacitors. For 741 IC, the maximum internal capacitor charging current is limited to about 15μA. So the slew rate of 741 IC is SR = dVc/dt |max = Imax/C For a sine wave input, the effect of slew rate can be calculated as consider volt follower. The input is large amp, high input, the effect of slew rate can be calculated as consider volt follower. The input is large amp, high frequency sine wave.

If Vs = Vm Sinwt then output V0 = Vm sinwt . The rate of change of output is given by dV0/dt=Vm w coswt.

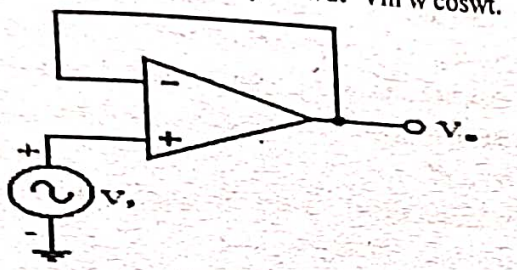


Fig. circuit diagram

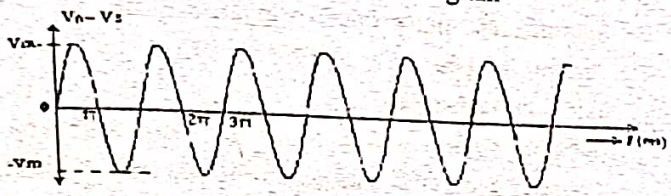


Fig. Wavefome

The max rate of change of output across when coswt=1 (i.e) SR = dV0/dt|max = wVm.

SR = 2 fVm V/s = 2fVm v/ms.

Thus the maximum frequency fmax at which undistorted output volt of peak value Vm is given by fmax (Hz) = Slew rate/6.28 * Vm called the full power response. It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

Q16. Explain Open - loop op-amp Configuration.?

Ans. The term open-loop indicates that no feedback in any form is fed to the input from the output. When connected in open – loop the op-amp functions as a very high gain amplifier. There are three open – loop configurations of op-amp namely,

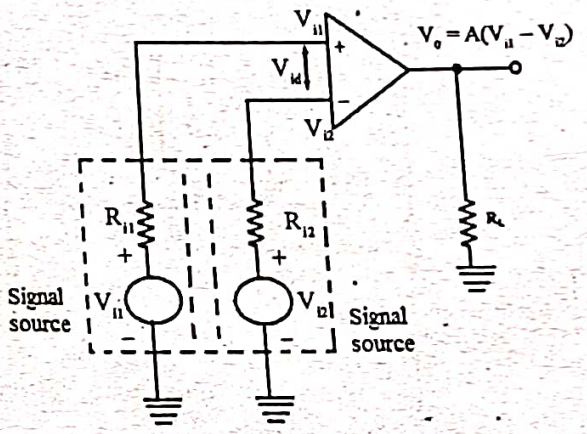
1. Differential amplifier
2. Inverting amplifier
3. Non-inverting amplifier

The above classification is made based on the number of inputs used and the terminal to which the input is applied. The op-amp amplifies both ac and dc input signals. Thus, the input signals can be either ac or dc voltage.

1. **Loop Differential Amplifier** : In this configuration, the inputs are applied to both the inverting and the non-inverting input terminals of the op-amp and it amplifies the difference between the two input voltages. Figure shows the open-loop differential amplifier configuration. The input voltages are represented by Vi_1 and Vi_2. The source resistance Ri_1 and Ri_2 are negligibly small in comparison with the very high input resistance offered by the op-amp, and thus the voltage drop across these source resistances is assumed to be zero. The output voltage V0 is given by

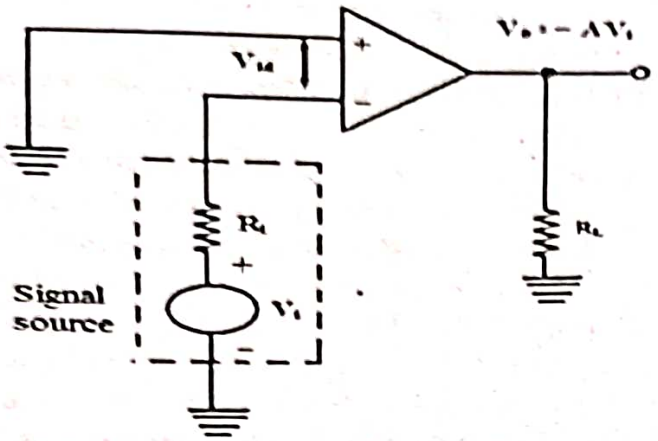
$$V_0 = A(V_{i1} - V_{i2})$$

where A is the large signal voltage gain. Thus the output voltage is equal to the voltage gain A times the difference between the two input voltages. This is the reason why this configuration is called a differential amplifier. In open – loop configurations, the large signal voltage gain A is also called open-loop gain A.



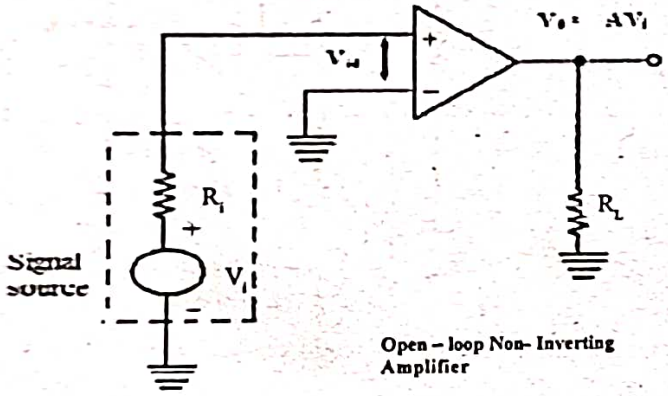
Open - loop Differential Amplifier

2. **Inverting amplifier :** In this configuration the input signal is applied to the inverting input terminal of the op- amp and the non-inverting input terminal is connected to the ground. Figure shows the circuit of an open – loop inverting amplifier. The output voltage is 180° out of phase with respect to the input and hence, the output voltage V_0 is given by, $V_0 = -AV_i$. Thus, in an inverting amplifier, the input signal is amplified by the open-loop gain A and is phase shifted by 180°.



Open - loop Inverting Amplifier

3. **Non-inverting Amplifier :** Figure shows the open – loop non- inverting amplifier. The input signal is applied to the non-inverting input terminal of the op-amp and the inverting input terminal is connected to the ground. The input signal is amplified by the open – loop gain A and the output is in-phase with input signal. $V_0 = AV_i$



Open – loop Non- Inverting Amplifier

In all the above open-loop configurations, only very small values of input voltages can be applied. Even for voltages levels slightly greater than zero, the output is driven into saturation, which is observed from the ideal transfer characteristics of op-amp shown in figure.

Q17. Explain Closed – loop op-amp configuration.

Ans. The op-amp can be effectively utilized in linear applications by providing a feedback from the output to the input, either directly or through another network. If the signal feedback is out- of-phase by 1800 with respect to the input, then the feedback is referred to as negative feedback or degenerative feedback. Conversely, if the feedback signal is in phase with that at the input, then the feedback is referred to as positive feedback or regenerative feedback. An op – amp that uses feedback is called a closed – loop amplifier. The most commonly used closed – loop amplifier configurations are :

1. Inverting amplifier (Voltage shunt amplifier)
2. Non- Inverting amplifier (Voltage – series Amplifier)

1. ***Inverting Amplifier:*** The inverting amplifier is shown in figure and its alternate circuit arrangement is shown in figure, with the circuit redrawn in a different way to illustrate how the voltage shunt feedback is achieved. The input signal drives the inverting input of the op – amp through resistor R1. The op – amp has an open – loop gain of A, so that the output signal is much larger than the error voltage. Because of the phase inversion, the output signal is 1800 out – of – phase with the input signal. This means that the feedback signal opposes the input signal and the feedback is negative or degenerative.

Practical Inverting amplifier : The practical inverting amplifier has finite value of input resistance and input current, its open voltage gain A_0 is less than infinity and its output resistance R_0 is not zero, as against the ideal inverting amplifier with finite input resistance, infinite open – loop voltage gain and zero output resistance respectively. Figure shows the low frequency equivalent circuit model of a practical inverting amplifier. This circuit can be simplified using the Thevenin's equivalent circuit shown in figure. The signal source Vi and the resistors R_1 and Ri are replaced by their Thevenin's equivalent values. The closed – loop gain AV and the input impedance Rif are calculated as follows. The input impedance of the op- amp is normally much larger than the input resistance R_1. Therefore, we can assume Veq $\approx$ Vi and Req $\approx R_1$. From the figure

$$V_0 = IR0 = AV_{id}$$
$$V_{id} = IR_f = AV_{id}$$
$$V_0 = IR_0 = AV_{id}$$

Substituting the 0 value f of I derived from above eqn. and obtaining the closed loop gain. It can be observed from above eqn. that when A>> 1, R_0 is negligibly small and the product $AR_1 >> R_0 + R_f$, the closed loop gain is given by

$$Av = -R_f / R_1$$

Which as the same form as given in above eqn for an ideal

inverter.

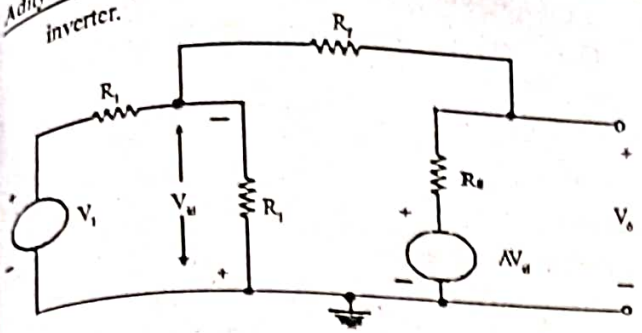
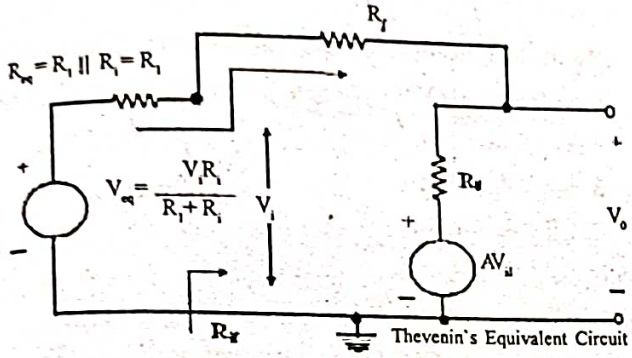


Fig. Equivalent Circuit of a Practical Inverting Amplifier

Input Resistance:

$R_{if} = V_{id} / I_1 = (R_f + R_0) / (1 + A)$



Thevenin's Equivalent Circuit

Output Resistance:

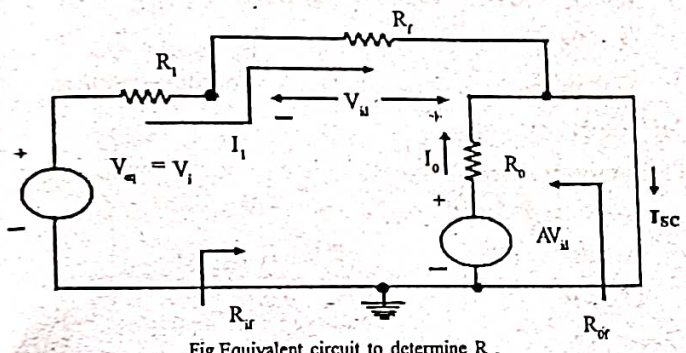
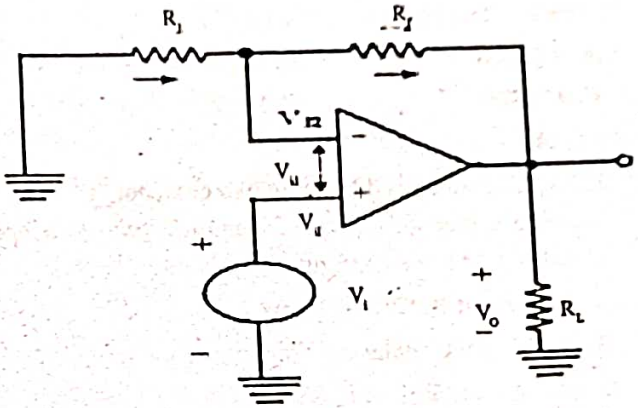


Fig.Equivalent circuit to determine R_{of}

Figure shows the equivalent circuit to determine Rof. The output impedance R_{of} without the load resistance factor R_L is calculated from the open circuit output voltage V_{oc} and the short circuit output current I_{SC}.

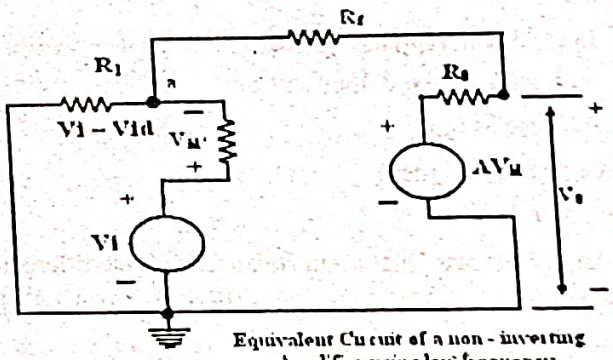
$$R_{of} = \frac{\dfrac{R_0(R_1 + R_f)}{R_0 + R_1 + R_f}}{1 + \dfrac{R_1 A}{R_0 + R_1 + R_f}}$$

2. *Non–Inverting Amplifier :* The non – inverting Amplifier with negative feedback is shown in figure. The input signal drives the non – inverting input of op-amp. The op-amp provides an internal gain A. The external resistors R_1 and Rf form the feedback voltage divider circuit with an attenuation factor of ß. Since the feedback voltage is at the inverting input, it opposes the input voltage at the non – inverting input terminals, and hence the feedback is negative or degenerative. The differential voltage V_{id} at the input of the op-amp is zero, because node A is at the same voltage as that of the non- inverting input terminal. As shown in figure, R_f and R_1 form a potential divider. Therefore,



Closed Loop Non – Inverting Amplifier : The input resistance of the op – amp is extremely large (approximately infinity,) since the op – amp draws negligible current from the input signal.

Practical Non –inverting amplifier : The equivalent circuit of a non- inverting amplifier using the low frequency model is shown below in figure. Using Kirchhoff's current law at node a,



Equivalent Circuit of a non - inverting Amplifier using low frequency

$$Av = 1 + \frac{R_f}{R_1}$$

OBJECTIVE QUESTIONS AND ANSWERS

1. A Differential Amplifier should have collector resistor's value (RC1 & RC2) as

   A. 5kΩ, 5kΩ B. 5Ω, 10kΩ
   C. 5Ω, 5kΩ D. 5kΩ, 10kΩ

Answer: a

2. A Differential Amplifier amplifies
   A. Input signal with higher voltage
   B. Input voltage with smaller voltage
   C. Sum of the input voltage
   D. None of the Mentioned

Answer: D

3. The value of emitter resistance in Emitter Biased circuit are RE1=25kΩ & RE2=16kΩ. Find RE

   A. 9.756kΩ B. 41kΩ
   C. 9.723kΩ D. 10kΩ

Answer: A

4. If output is measured between two collectors of transistors, then the Differential amplifier with two input signal is said to be configured as
   A. Dual Input Balanced Output
   B. Dual Input Unbalanced Output
   C. Single Input Balanced Output
   D. Dual Input Unbalanced Output

Answer: A

5. A differential amplifier is capable of amplifying
   A. DC input signal only
   B. AC input signal only
   C. AC & DC input signal
   D. None of the Mentioned

Answer: C

6. In ideal Differential Amplifier, if same signal is given to both inputs, then output will be

   A. Same as input B. Double the input
   C. Not equal to zero D. Zero

Answer: D

7. An emitter bias Dual Input Balanced Output differential amplifier has VCC=20v, β=100, VBE=0.7v, RE=1.3kΩ. Find IE

   A. 7.42mA B. 9.8mA
   C. 10mA D. 8.6mA

Answer: A

8. Find IC, given VCE=0.77v, VCC=10v, VBE=0.37v and RC=2.4kΩ in Dual Input Balanced Output differential amplifier

   A. 0.4mA B. 0.4A
   C. 4mA D. 4A

Answer: C

9. Find the correct match

Configuration	Voltage gain and Input resistance
1. Single Input Unbalanced Output	i. $A_d = Rc/re$, R_{i1} $R_{i2} = 2\beta_{ac}R_E$
2. Dual Input Balanced Output	ii. $A_d = Rc/2re$, $Ri1$ $Ri2 = 2\beta_{ac}R_E$
3. Single Input Balanced Output	iii. $A_d = Rc/re$, $R_i = 2\beta_{ac}RE$
4. Dual Input Unbalanced Output	iv. $A_d = Rc/2re$, $R_i = 2\beta_{ac}RE$

   A. 1-i, 2-iii, 3-iv, 4-ii
   B. 1-iv, 2-ii, 3-iii, 4-i
   C. 1-ii, 2-iv, 3-i, 4-iii
   D. 1-iii, 2-i, 3-ii, 4-iv

Answer: D

10. Obtain the collector voltage, for collector resistor (RC =5.6kΩ, IE=1.664mA and VCC=10v for single input unbalanced output differential amplifier

    A. 0.987v B. 0.682v
    C. 0.555v D. None of the mentioned

Answer: B

11. For the circuit shown below, determine the Output voltage (Assume β=5, differential input resistance=12 kΩ)

    A. 4.33v B. 2.33v
    C. 3.33v D. 1.33v

Answer: C

12. In a Single Input Balanced Output Differential amplifier, given VCC=15v, RE=3.9kΩ, VCE=2.4 v and re=250Ω. Determine Voltage gain

    A. 26 B. 56
    C. 38 D. 61

Answer: A

13. The process involved in photolithography is
    a) Making of a photographic mask only
    b) Photo etching

c) Both photo etching and making of photographic mask
d) None of the mentioned

Answer: c

14. How will be the initial artwork done for a normal IC?
a) Smaller than the final dimension of chip
b) Same as that of final dimension of chip
c) Larger than the final dimension of chip
d) None of the mentioned

Answer: c

15. Find the area of artwork done for a monolithic chip of area 30mil × 30mil.
a) 16 cm × 16 cm
b) 60 cm × 60 cm
c) 12 cm × 12 cm
d) 36 cm × 36 cm

Answer: d

16. Mylar coated with a sheet of red photographic Mylar is used for artwork (layout) because,
a) It is used to get a colourful layout
b) It can be easily peeled off from layout
c) It is recommended colour for layouts
d) It is used for highlighting layout

Answer: b

17. Find the coating material used for photo etching process along with its thickness range.
a) Kodak photoresist (5000-10000Å)
b) Kodak photoresist (1000-5000Å)
c) Kodak photo etchant (1000-5000 Å)
d) Kodak photo etchant (500-1000 Å)

Answer: a

18. Which type of etching process is preferred to make the photoresist immune to etchants?
a) None of the mentioned
b) Wet etching
c) Plasma etching
d) Chemical etching

Answer: c

19. Which of the following statement is not true?
a) X-ray and Electron beam lithography technique, produce device dimensions down to submicron range.
b) Ultraviolet lithography has limitation due to diffraction effects of wavelength.
c) The cost of X-ray or Electron beam is less compared to Ultraviolet photolithography.
d) The exposure time is less in Ultraviolet compared to X-ray or Electron beam lithography.

Answer: c

20. For photographic purpose usually coordinatograph is preferred for artwork because,
a) It is a precision drafting machine
b) Cutting head can be positioned accurately
c) It can be moved along two perpendicular axes
d) All of the mentioned

Answer: d

21. Which of the following is added as an impurity to p-type material in diffusion process?
a) Phosphorous pentaoxide (P_2O_5)
b) Phosphorous oxychloride ($POcl_3$)
c) Boron oxide (B_2O_3)
d) None of the mentioned

Answer: c

22. In the fabrication of monolithic ICs, Boron chloride is added as an impurity in the diffusion process. Find the diffusion time, if the furnace is heated up to 1200°c.
a) 1 hour
b) 2 hours
c) 45 minutes
d) 30 minutes

Answer: b

UNIT 02

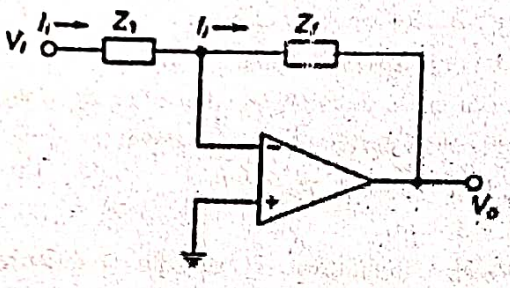
APPLICATIONS OF OPERATIONAL AMPLIFIERS

QUESTIONS AND ANSWERS

Q1. Explain the terms :

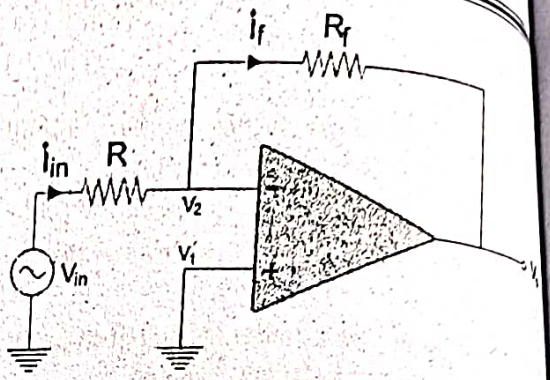
1. **Sign Changer (Phase Inverter).**
2. **Scale Changer.**
3. **Phase Shift Circuits.**
4. **Voltage Follower.**

1. Sign Changer (Phase Inverter) :



The basic inverting amplifier configuration using an op-amp with input impedance Z_1 and feedback impedance Z_f. If the impedance Z_1 and Z_f are equal in magnitude° and phase, then the closed loop voltage gain is -1, and the input signal will undergo a 180 phase shift at the output. Hence, such circuit is also called phase inverter. If two such amplifiers are connected in cascade, then the output from the second stage is the same as the input signal without any change of sign. Hence, the outputs from the two stages are equal in magnitude but opposite in phase and such a system is an excellent paraphase amplifier.

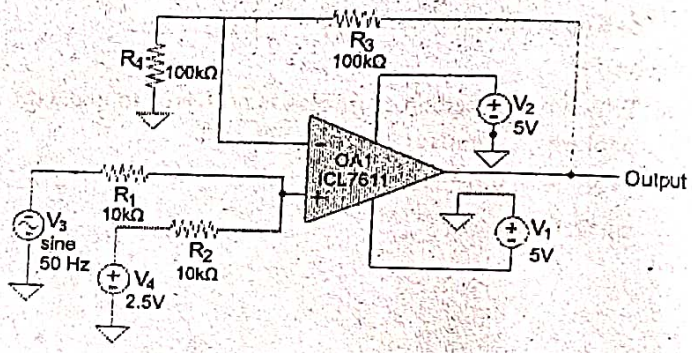
2. Scale Changer : Op-Amp functions as a scale changer through small signals with constant-gain in both inverting and non-inverting amplifiers.



Non-inverting terminal is grounded whereas R1 links the input signal v_1 to the inverting input. A feedback resistor R_f is then connected from output to the inverting input. The closed loop gain of the inverting amplifier works based on the ratio of the two external resistors R_1 and R_f and Op-Amp acts as a negative scaler when it multiplies the input by a negative constant factor.

While in need for an output that is equal to input for getting multiplied by a positive constant the positive scaler circuit is used by applying negative feedback.

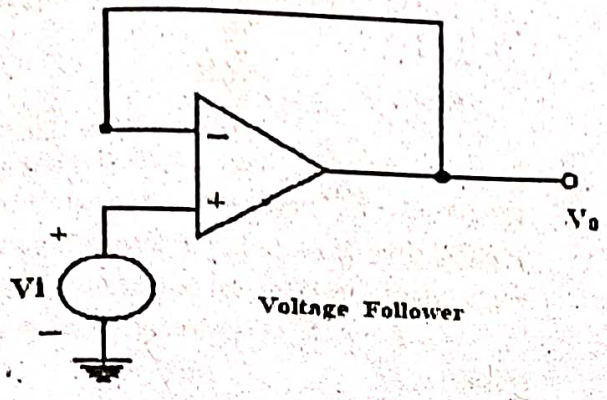
3. Phase Shifter circuit :



Op-Amp is used for direct coupling procedure and so DC voltage level at the emitter terminal increases from phase to phase. This rapidly increasing DC level is likely to shift the operating point of the upcoming stages. Thus to move

down the increasing voltage swing, this phase shifter is applied.The phase shifter performs by adding a DC voltage level to the output of fall stage to pass the output to a ground level.

4. **Voltage Follower :** If $R_1 = 8$ and $R_f = 0$ in the non inverting amplifier configuration. The amplifier act as a unity-gain amplifier or voltage follower.

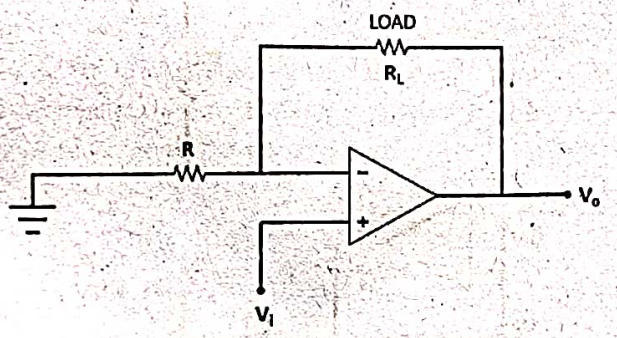


Voltage Follower

The circuit consists of an op -amp and a wire connecting the output voltage to the input, i.e. the output voltagev is equal to the input voltage, both in magnitude and phase. V0 = Vi.Since the output voltage of the circuit follows the input voltage, the circuit is called voltage follower. It offers very high input impedance of the order of M and very low output impedance.Therefore, this circuit draws negligible current from the source. Thus, the voltage follower can be used as a buffer between a high impedance source and a low impedance load for impedance matching applications.

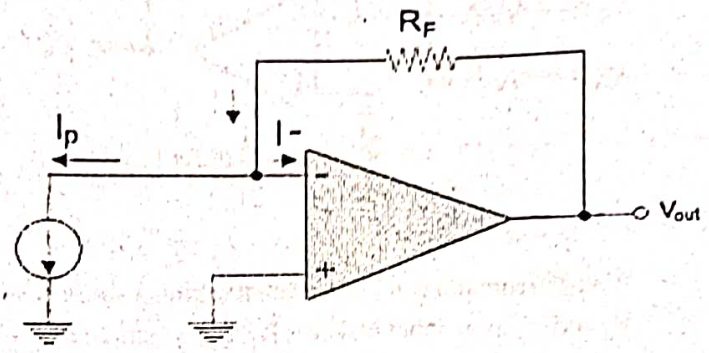
Q2. Explain Voltage to Current (V- to - I) and Current to Voltage (I - to - V) converters.

Ans.Voltage to Current Converter :



An op-amp with a negative feedback is generally used for voltage to current conversions. Below you can see the circuit diagram. We are not going into the details here, just we will discuss the circuit given below. The voltage is applied to the non-inverting terminal and the output is feedback to the inverting terminal. It is also grounded using a resistor.

Current to Voltage Converter :



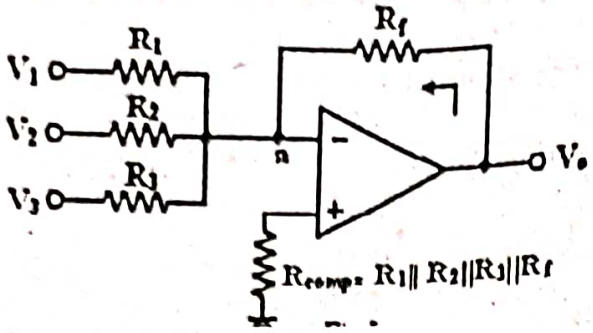
Op-amp can be used as a current to voltage converter using a very simple circuit as shown above. All we need is a feedback resistance connected to the output of the op-amp. The current source is fed into the inverting terminal and the non-inverting terminal is grounded. Here the output voltage is proportional to the input current. As an ideal op-amp has infinite resistance, the current cannot flow through the op-amp. The current flows through the feedback resistance and the voltage across it depends on the current source.

Q3. Explain the Op Amp application as a :-

1. **Adder**
2. **Subtractor**
3. **Instrumentation amplifier**
4. **Integrator**
5. **Differentiator**
6. **Logarithmic amplifier**
7. **Antilogarithmic amplifier**
8. **Comparators**
9. **Schmitt trigger**
10. **Precision rectifier**
11. **Peak detector**

1. **Adder :** Op-amp may be used to design a circuit whose output is the sum of several input signals.Such a ircuit is called a summing amplifier or a summer or adder. An inverting summer or a non-inverting summer may be discussed now.

Inverting Summing Amplifier:



A typical summing amplifier with three input voltages V1, V_2 and V_3 three input resistors R_1, R_2, R_3 and a feedback resistor Rf is shown in figure .The following analysis is carried out assuming that the op-amp is an ideal one, AOL= S.Since the input bias current is assumed to be zero, there is no voltage drop across the resistor Rcomp and hence the non-inverting input terminal is at ground potential.

$I = V_1/R_1 + V_2/R_2 ..... + Vn/Rn;$

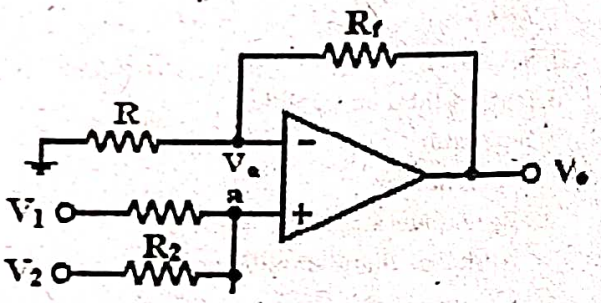
$Vo = - RfI = Rf/R\,(V_1 + V_2 + ... Vn).$

To find Rcomp, make all inputs $V_1 = V_2 = V_3 = 0$.

So the effective input resistance $Ri = R_1 \| R_2 \| R_3$.

Therefore, $Rcomp = Ri \| Rf = R_1 \| R_2 \| R_3 \| R,f$.

Non-Inverting Summing Amplifier:



A summer that gives a non-inverted sum is the non-inverting summing amplifier of figure Let the voltage at the (–) input terminal be Va. which is a non-inverting weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R\,f/2$, then $Vo = V_1 + V_2 + V_3$.

2. ***Subtractor :*** A basic differential amplifier can be used as a subtractor as shown in the above figure. If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

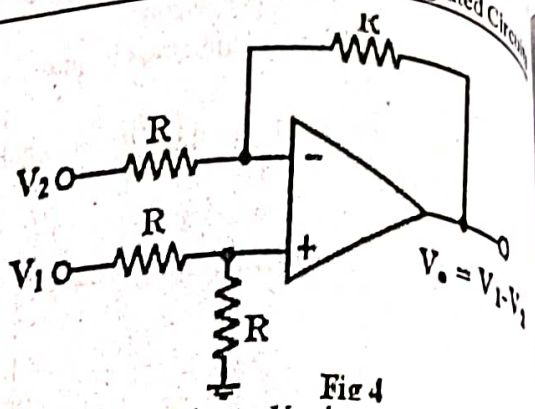


Fig 4

To find the output V_{01} due to V_1 alone, make $V_2 = 0$. Then the circuit of figure as shown in the above becomes a non-inverting amplifier having input voltage V1/2 at the non-inverting input terminal and the output becomes $V_{01} = V1/2(1 + R/R) = V_1$ when all resistances are R in the circuit.

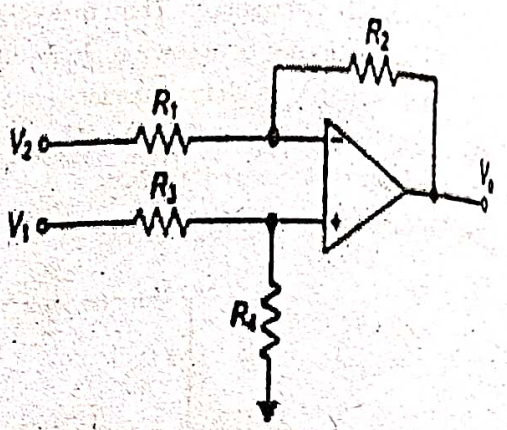
Similarly the output V_{02} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

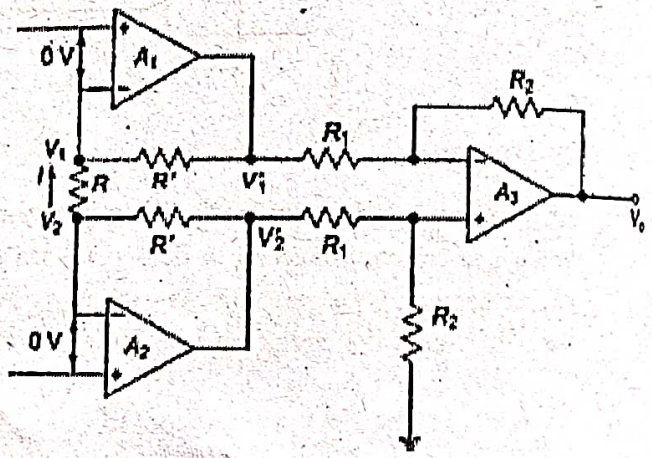
$$V_{02} = -V_2$$

Thus the output voltage Vo due to both the inputs can be written as

$$V_0 = V_{01} - V_{02} = V_1 - V_2$$

3. **Instrumentation amplifier :**





Current flowing in resistor R is I= $(V_1 - V_2)/R$ and it flow through R' in the direction shown, Voltage at non-inverting terminal op-amp A_3 is $R_2 V1'/(R_1+R_2)$. By superposition theorem

$$Vo = (R_2/R_1)V_1 + (1+R_2/R_1)(R_2V_2/(R_1+R_2)$$
$$= R_2/R1(V1'-V2');$$
$$V1' = R'I + V_1 = R'/R(V_1 - V_2) + V1$$
$$V2' = R'I + V_1 = R'/R(V_1 - V_2) + V_2;$$
$$V0 = (R_2/R_1)[(2R'/R(V_2 - V_1) + (V_2 - V_1)]$$
$$= (R_2/R_1)[(1+2R'/R)(V_2 - V1)$$

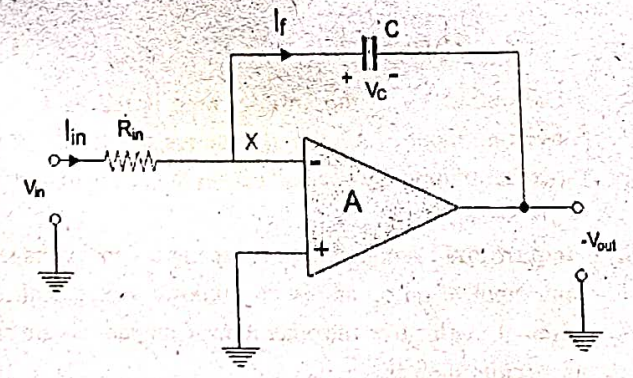
In a number of industrial and consumer applications, one is required to measure and control physical quantities. Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. these physical quantities are usually measured with help of transducers. he output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier. The important features of an instrumentation amplifier are

1. High gain accuracy
2. High CMRR
3. High gain stability with low temperature coefficient
4. Low output impedance

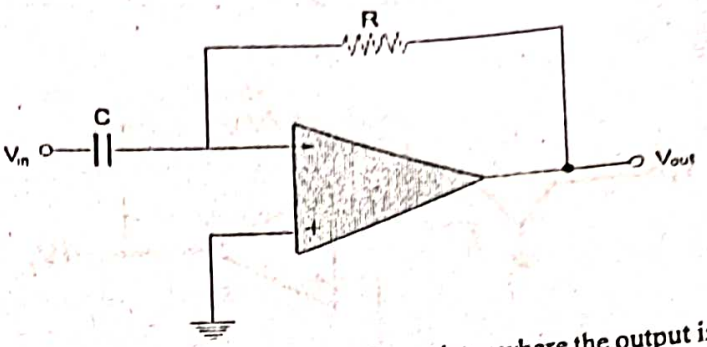
Applications of instrumentation amplifier with the transducer bridge,

- o temperature indicator,
- o temperature controller and
- o light intensity meter

4. **Integrator :** Op-amp is used as an integrator also. The integrator op-amp produces an output that is proportional to the amplitude of the input signal as well as the duration of the input signal. Instead of a resistor in the feedback loop, we have a capacitor. It is able to perform the mathematical operation of integration as the output varies with the input and duration of the signal.



5. Differentiator :

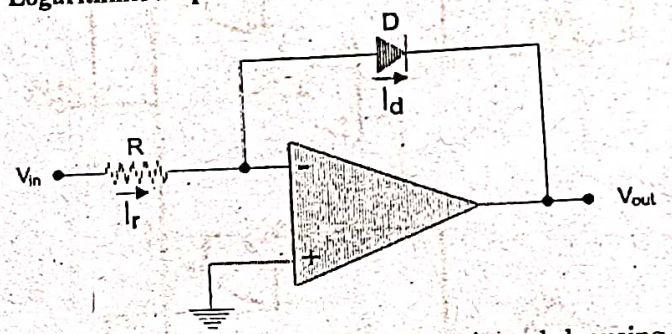


Op-amp can be used as a differentiator where the output is the first derivative of the input signal. The following equation gives the relation between the input signal and the output signal.

$$V_{OUT} = -R_F C \frac{dV_{IN}}{dt}$$

As you can see the output voltage is a first derivative of the input voltage. We are not going into how the equation is derived but only learning about the use of an op amp as a differentiator.

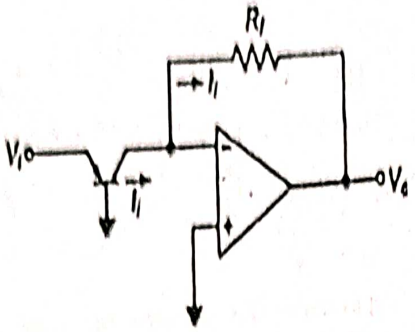
6. **Logarithmic amplifier :**



The logarithmic amplifier using op-amp is made by using a diode instead of a resistance in the feedback loop. The non-inverting terminal is grounded and the input voltage is fed to the inverting terminal. The output voltage is proportional to the logarithm of the input voltage and hence can be used as a logarithmic amplifier.

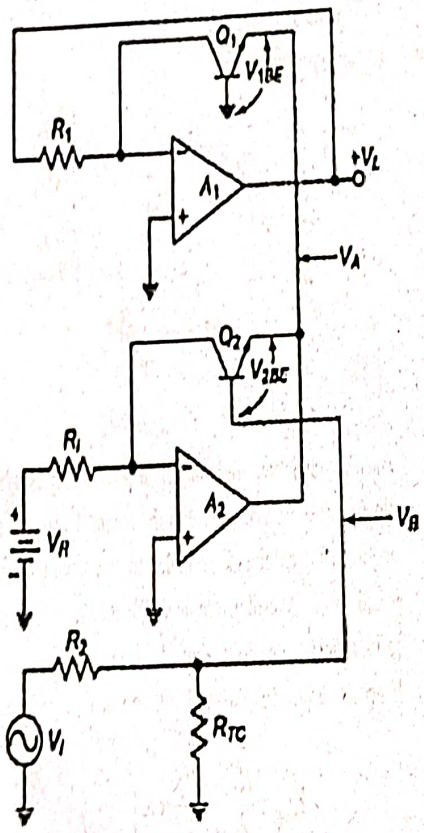
$$V_{out} = \frac{KT}{Q} \times \left(\frac{V_{in}}{I_r} \times R \right)$$

7. **Antilogarithmic amplifier :** A circuit to convert logarithmically encoded signal to real signals. Transistor in inverting input converts input voltage into logarithmically varying currents.



$I_i = I_e = I_s(e^{\frac{\eta V_{BE}}{kT}})$ and $V_0 = R_f I_s(e^{\frac{\eta V_{BE}}{kT}})$

The circuit is shown in figure below. The input Vi for the antilog-amp is fed into the temperature compensating voltage divider R_2 and RTC and then to the base of Q_2. The output of A_2 is fed back to R_1 at the inverting input of op amp A_1. The non-inverting inputs are grounded



$$V_{1BE} = \frac{kT}{q}\ln\left[\frac{V_L}{R_1 I_s}\right] \text{ and } V_{2BE} = \frac{kT}{q}\left[\frac{V_B}{R_1 I_s}\right]$$

and $V_A = -V_{1BE}$ and $V_B = R_{TC}/(R_2 + R_{TC})V_I$

$$V_{Q2E} = V_B + V_{2BE} = R_{TC}/(R_2 + R_{TC})V_I - \frac{kT}{q}\ln\left[\frac{V_B}{R_1 I_s}\right]$$

$V_{Q2E} = V_A$

Therefore,

$$-\frac{kT}{q}\ln\left(\frac{V_L}{R_1 I_s}\right) = \frac{R_{TC}}{R_2 + R_{TC}}V_I + \frac{kT}{q}\ln\left(\frac{V_R}{R_1 I_s}\right)$$

Rearranging, we get

$$\frac{R_{TC}}{R_2 + R_{TC}}V_I = -\frac{kT}{q}\ln\left(\frac{V_L}{R_1 I_s}\right) - \frac{kT}{q}\ln\left(\frac{V_R}{R_1 I_s}\right)$$

$$= -\frac{kT}{q}\ln\left(\frac{V_L}{V_R}\right)$$

We know that $\log_{10} x = 0.4343 \ln x$.

Therefore,

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_I = 0.4343\ln\left(\frac{V_L}{V_R}\right)$$

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_I = \log_{10}\left(\frac{V_L}{V_R}\right)$$

$$-KV_r = \log\left(\frac{V_L}{V_R}\right)$$

$$K = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

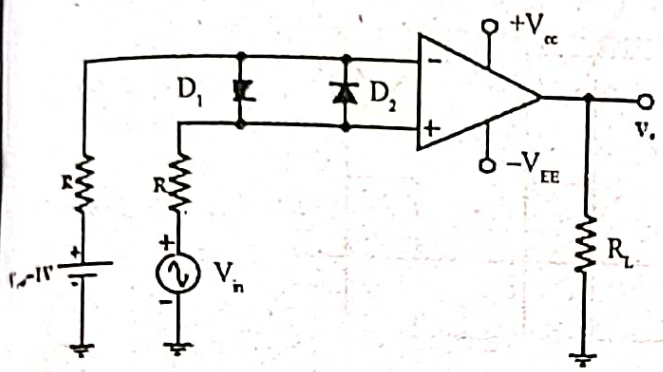
$$V_L = V_R 10^{-kV_r}$$

The output Vo of the antilog- amp is fed back to the inverting input of A1 through the resistor R1. Hence an increase of input by one volt causes the output to decrease by a decade.

8. **Comparators :** A comparator compares a signal voltage o one input of an op-amp with a known voltage called reference voltage on the other input. Comparators are us in circuits such as,

- Digital Interfacing
- Discriminator
- Schmitt Trigger
- Voltage level detector and oscillators

Non-inverting Comparator:



A fixed reference voltage V_{ref} of 1 V is applied to the negative terminal and time varying signal voltage V_{in} is applied to the positive terminal. When V_{in} is less than Vref the output becomes V_0 at $-V_{sat}$

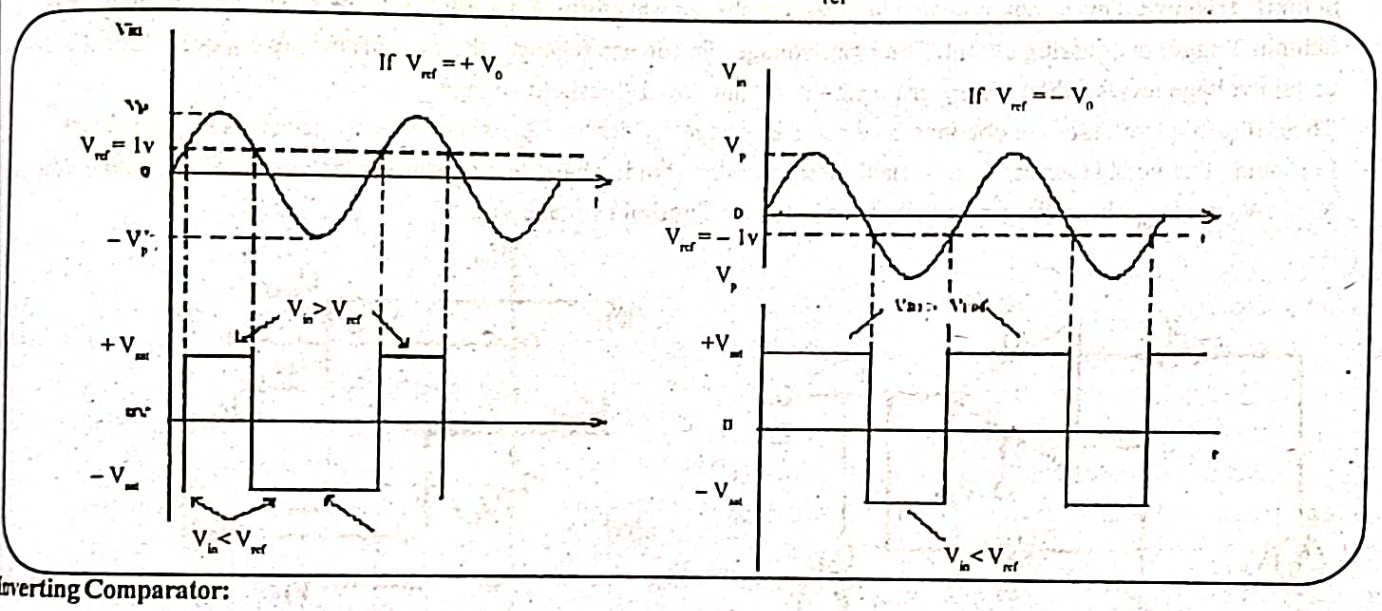
$$[V_{in} < V_{ref} \Rightarrow V_0(-V_{sat})].$$

When V_{in} is greater than V_{ref}, the (+) input becomes positive, the V0 goes to +Vsat.

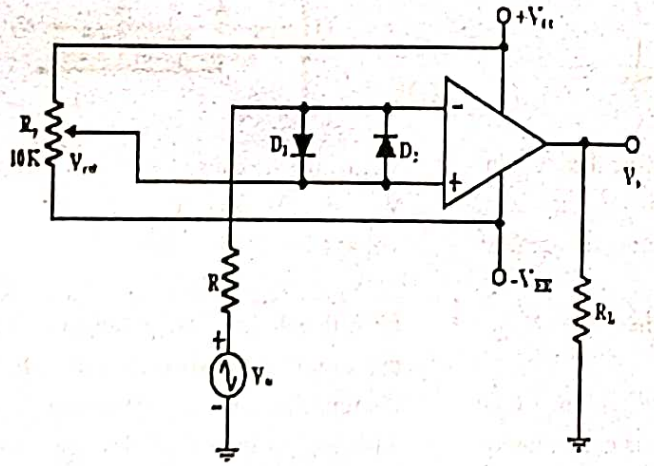
$$[V_{in} > V_{ref} \Rightarrow V_0(+V_{sat})].$$

Thus the V_0 changes from one saturation level to another.The diodes D_1 and D_2 protect the op-amp from damage due to the excessive input voltage V_{in}. Because of these diodes, the difference input voltage Vid of the op-amp diodes are called clamp diodes

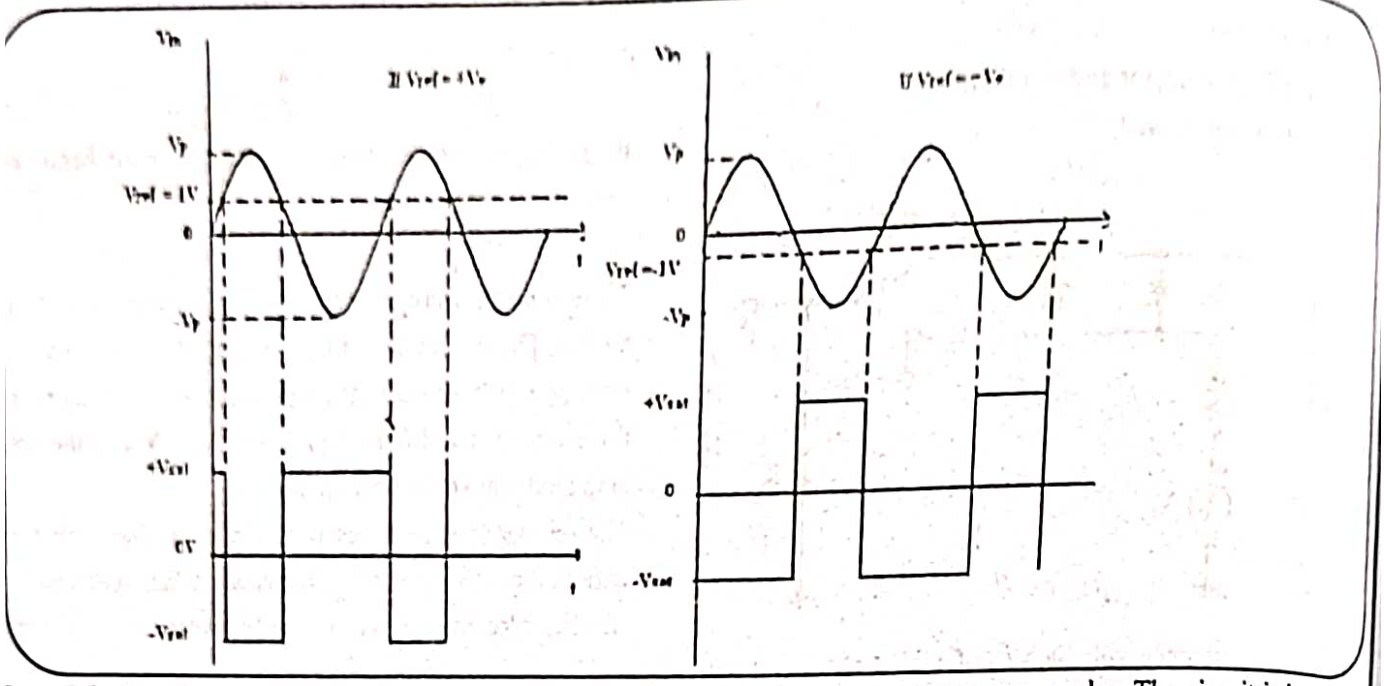
The resistance R in series with Vin is used to limit the current through D_1 and D_2. To reduce offset problems, a resistance Rcomp = R is connected between the (-ve) input and V_{ref}



Inverting Comparator:

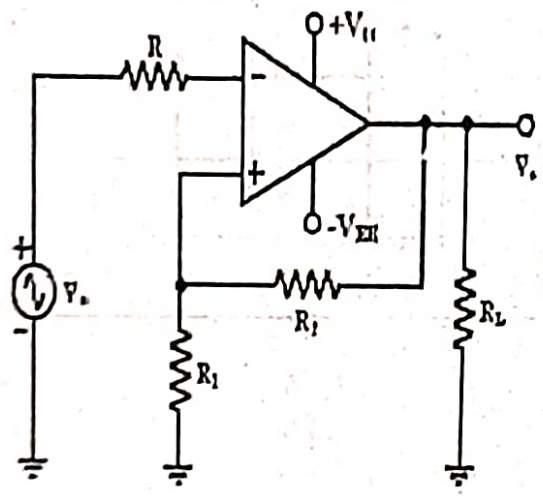


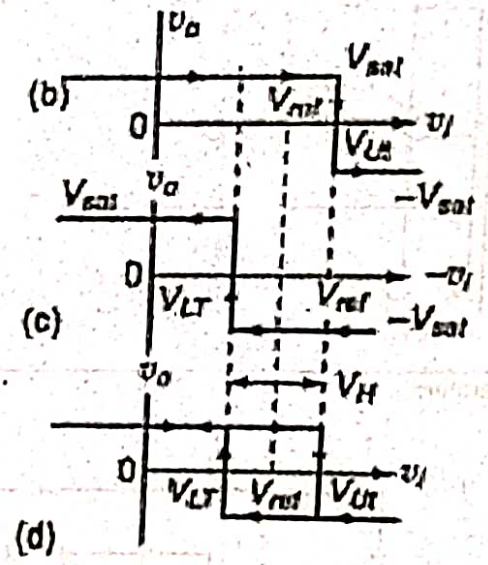
desired amplitude and polarity can be got by simply adjusting the 10k potentiometer.



9. **Schmitt trigger :** This circuit converts an irregular shaped waveform to a square wave or pulse. The circuit is known as Schmitt Trigger or squaring circuit. The input voltage Vin triggers (changes the state of) the o/p V_0 every time it exceeds certain voltage levels called the upper threshold Vut and lower threshold voltage.

These threshold voltages are obtained by using the voltage divider $R_1 - R_2$, where the voltage across R_1 is feedback to the (+) input. The voltage across R_1 is variable reference threshold voltage that depends on the value of the output voltage. When $V_0 = +V_{sat}$, the voltage across R_1 is called upper threshold voltage Vut.





The input voltage Vin must be more positive than V_{ut} in order to cause the output V_0 to switch from $+V_{sat}$ to $-V_{sat}$ using voltage divider rule, Voltage at (+) input terminal is

$$V_{UT} = V_{ref} + R_2 (V_{sat} - V_{ref}) / (R_1 + R_2)$$

when $V_0 = +V_{sat}$.

When $v_0 = -V_{sat}$.

Hysteris width $VH = V_{UT} - V_{LT} = 2 R_2 (V_{sat}) / (R_1 + R_2)$

When $V_0 = -V_{sat}$, the voltage across R_1 is called lower threshold voltage V_{lt} .the V_{in} must be more negative than V_{lt} in order to cause V_0 to switch from $-V_{sat}$ to $+V_{sat}$. for $V_{in} > V_{lt}$, V_0 is at $-V_{sat}$.

Voltage at (+) terminal is

$$V_{LT} = V_{ref} - R_2 (V_{sat} + V_{ref}) / (R_1 + R_2).$$

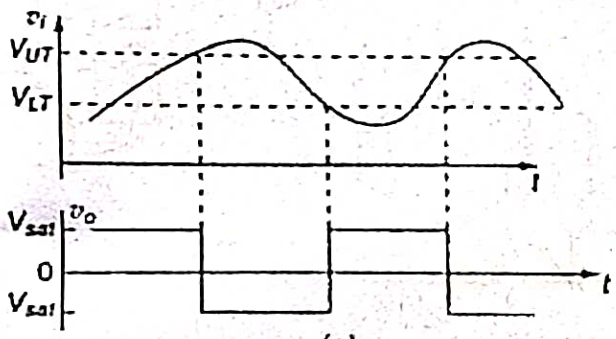
If the threshold voltages Vut and Vlt are made larger than the input noise voltages, the positive feedback will eliminate the false o/p transitions.

Also the positive feedback, because of its regenerative action, will make V_0 switch faster between $+V_{sat}$ and -

V_{sat}.

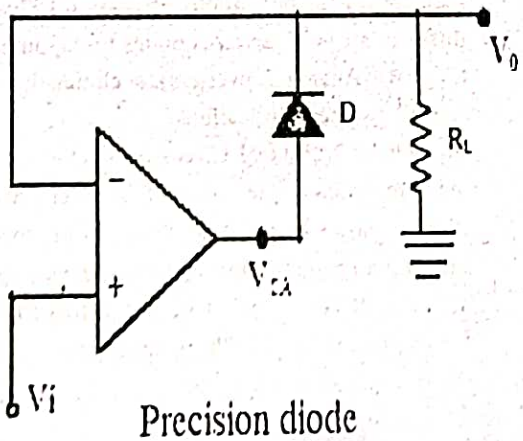
- Resistance Rcomp=$R_1 \| R_2$ is used to minimize the offset problems.
- The comparator with positive feedback is said to exhibit hysteresis, a dead band condition. (i.e) when the input of the comparator exceeds Vut its output switches from $+V_{sat}$ to $-V_{sat}$ and reverts to its original state, $+V_{sat}$ when the input goes below V_{LT}. The hysteresis voltage is equal to the difference between V_{ut} and V_{lt}. Therefore

  $V_H = V_{ut} - V_{lt}$.
- If $V_{ref} = 0$, $V_{ut} = -VLT = 2R_2(V_{sat})/(R_1+R_2)$

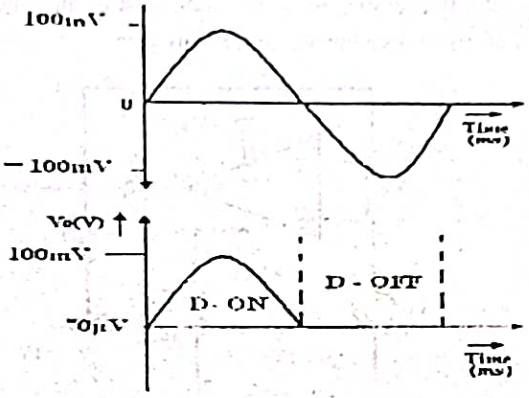


(e)

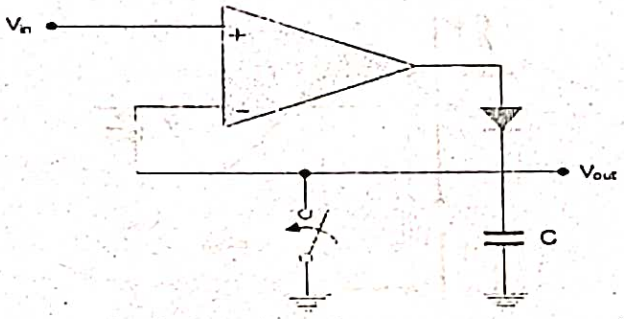
10. Precision rectifier : The ordinary diodes cannot rectify voltages below the cut-in -voltage of the diode. A circuit which can act as an ideal diode or precision signal – processing rectifier circuit for rectifying voltages which are below the level of cut-in voltage of the diode can be designed by placing the diode in the feedback loop of an op-amp.



Precision diode



II. **Peak detector :**



The circuit above shows the use of op-amp as a peak detector. The circuit uses a diode and a capacitor. When Vout is more than Vin, the output is positive and the diode conducts. Whereas when Vout is less than Vin, the diode is reversed biased and does not conduct. The capacitor charges to the most positive value.

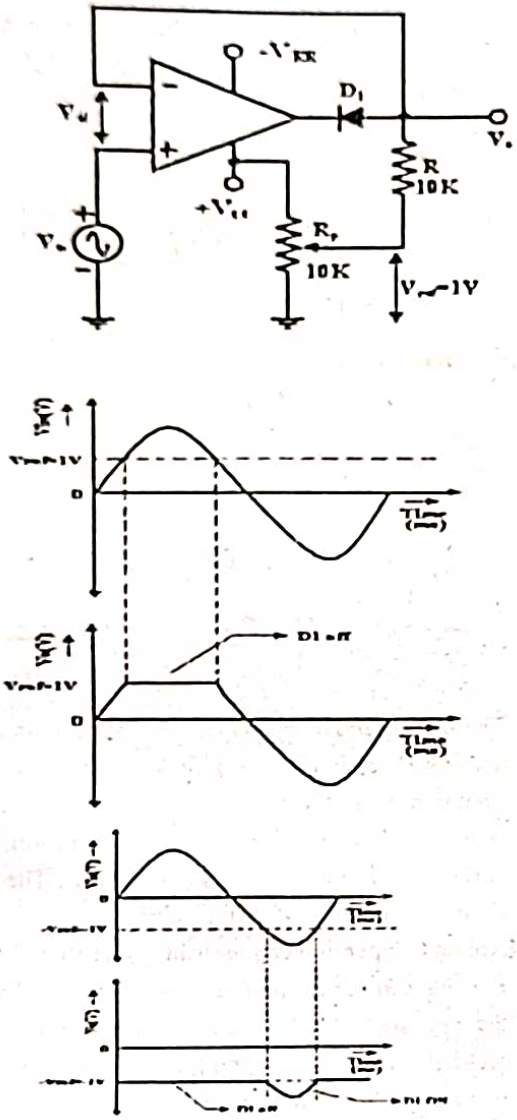
Q4. Explain Clipper and clipper using Operational Amplifier.

Ans. ***Positive Clipper :*** circuit that removes positive parts of the input signal can be formed by using an op-amp with a rectifier diode. T he clipping level is determined by the reference voltage Vref, which should less than the i/p range of the op-amp (Vref < Vin). The Output voltage has the portions of the positive half cycles aboye Vref clipped off.

The circuit works as follows: During the positive half cycle of the input, the diode D1 conducts only until Vin = Vref. This happens because when Vin <Vref, the output volts V0 of the op-amp becomes negative to device D1 into conduction when D1 conducts it closes feedback loop and op-amp operates as a voltage follower. (i.e.) Output V0 follows input until Vin = Vref. When Vin > Vref => the V0 becomes +ve to derive D1 into off.

The op-amp alternates between open loop (off) and closed loop operation as the D_1 is turned off and on respectively.

For this reason the op-amp used must be high speed and preferably compensated for unity gain.

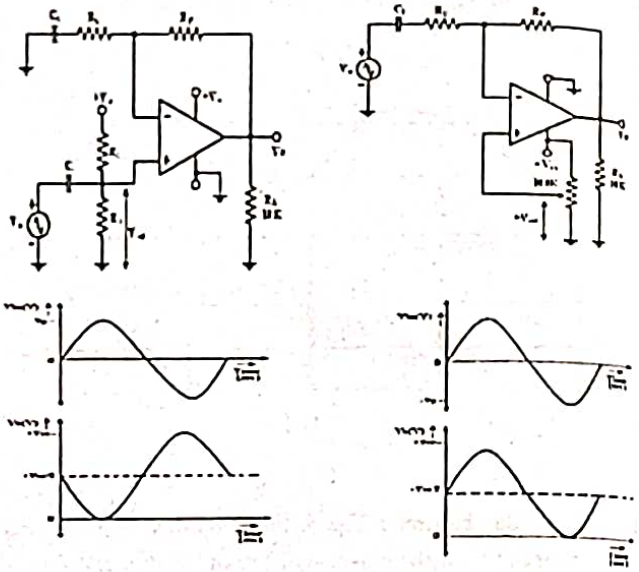


Negative Clipper: The positive clipper is converted into a –ve clipper by simply reversing diode D1 and changing the polarity of Vref voltage. The negative clipper clips off the –ve parts of the input signal below the reference voltage. Diode D1 conducts -> when Vin > –Vref and therefore during this period o/p volt V0 follows the i/p volt Vin. The –Ve portion of the output volt below –Vref is clipped off because (D1 is off) Vin<-Vref. If–Vref is changed to –Vref by connecting the potentiometer Rp to the +Vcc, the V0 below + Vref will be clipped off. The diode D1 must be on for Vin > Vref and off for Vin.

Positive and Negative Clampers: In clamper circuits a predetermined dc level is added to the output voltage (or) The output is clamped to a desired dc level.

1. If the clamped dc level is +ve, the clamper is positive clamper
2. If the clamped dc level is –ve, the clamper is negative clamper.

Other equivalent terms used for clamper are dc inserter or restorer. Inverting and Non-Inverting that uses this technique.

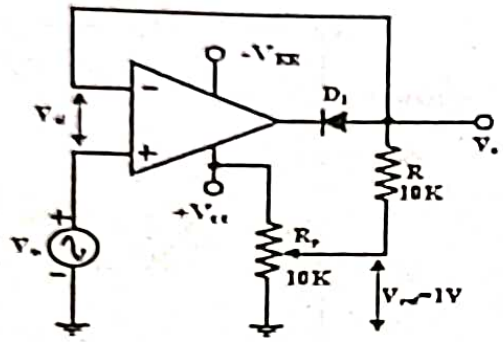


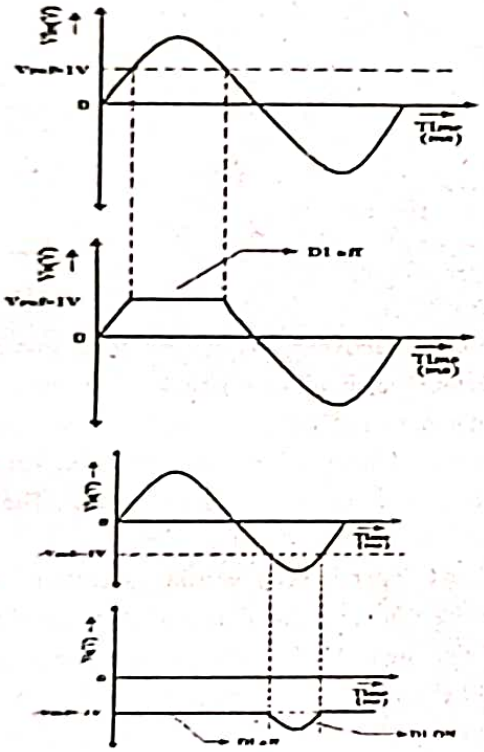
Q5. Explain Low Pass Filter Using Op Amp.

Ans. Op-Amps or operational amplifiers supply very efficient low pass filters without using inductors. The feedback loop of an op-amp can be incorporated with the basic elements of a filter, so the high-performance LPFs are easily formed by using the required components except for inductors. The applications of op-amp LPFs are used in different areas of power supplies to the outputs of DAC (Digital to Analog Converters) for eliminating alias signals as well as other applications.

First Order Active LPF Circuit using Op-Amp : The circuit diagram of the single pole or first order active low pass filter is shown below. The circuit of the low pass filter using op-amp uses a capacitor across the feedback resistor. This circuit has an effect when the frequency increases for enhancing the feedback level then the capacitor's reactive impedance falls.

For this reason the op-amp used must be high speed and preferably compensated for unity gain.





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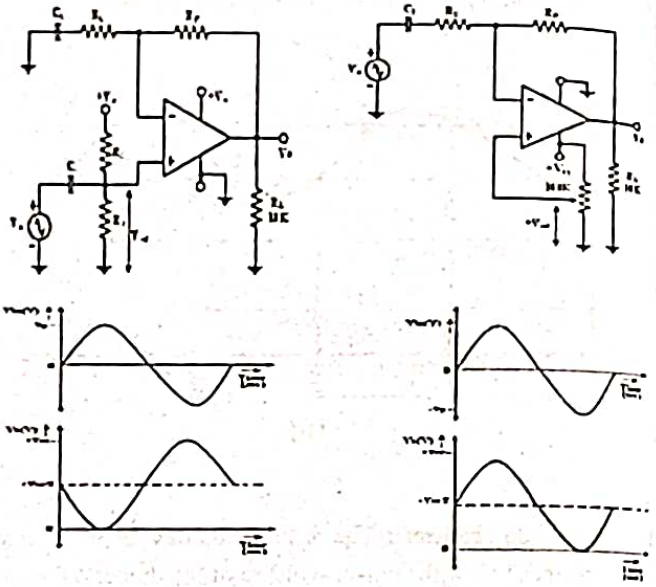

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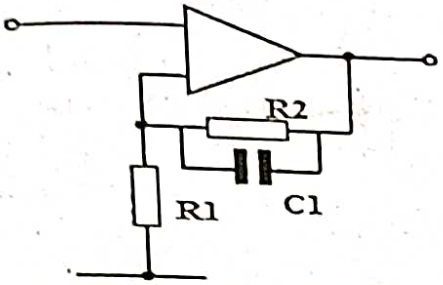
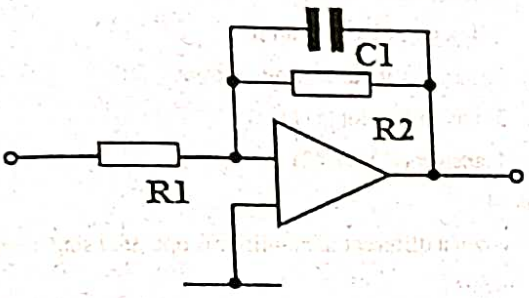


Non Inverting Configuration



Inverting Configuration

Fig. First Order Low Pass Filter Using Op Amp

The calculation of this filter can be done by working on the frequency at which the capacitor reactance can equal the resistance of the resistor. This can be obtained by using the following formula.

$$Xc = 1/p\,f\,C$$

Where 'Xc' is the capacitive reactance in ohms

'p' is the standard letter and the value of this is 3.412

'f' is the frequency (Units-Hz)

'C' is the capacitance (Units-Farads)

The in-band gain of these circuits can be calculated in a simple way by eliminating the capacitor's effect. As these types of circuits are helpful to give a reduction within gain at high frequencies, as well as offers an ultimate speed for roll-off of 6 dB for each octave, which means the o/p voltage divides for each repetition in frequency. So, this kind of filter is named as first order or single pole low pass filter

Second Order Active LPF Circuit using Op-Amp: By using an operational amplifier, it is possible for designing filters in a wide range with dissimilar gain levels as well as roll-off models. This filter offers a bandwidth response as well as unity gain.

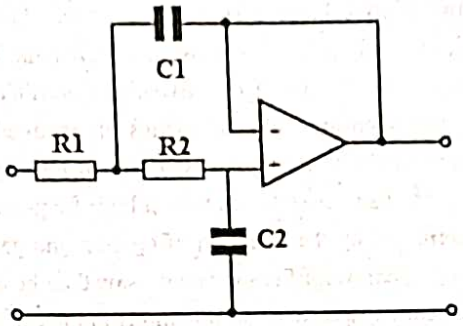


Fig. Second Order Active LPF Circuit using Op-Amp

The circuit values calculations are uncomplicated for the response of Butterworth low pass filter & unity gain. Significant damping is necessary for these circuits & the ratio values of the capacitor and resistor conclude this.

R1 = R2

C1 = C2

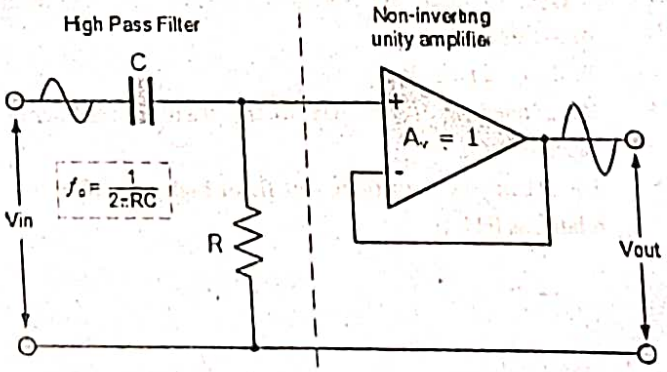
$$f = 1 - \sqrt{4\,p\,R\,C2}$$

While selecting the values, make sure that the values of the resistor will drop in the region among 10 kilos ohm to 100 kilo-ohms. This is worthwhile as the circuit's o/p impedance increases by the frequency & outside values of this section may change the act.

Q6. Define Active High Pass Filter (HPF).

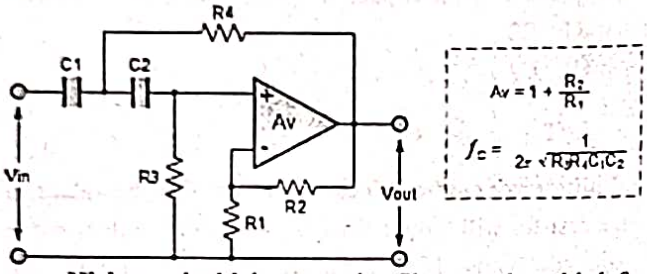
Ans. The basic operation of an Active High Pass Filter (HPF) is the same as for its equivalent RC passive high pass filter circuit, except this time the circuit has an operational amplifier or included within its design providing amplification and gain control. Like the previous active low pass filter circuit, the simplest form of an active high pass filter is to connect a standard inverting or non-inverting operational amplifier to the basic RC high pass passive filter circuit as shown.

First Order High Pass Filter :



Technically, there is no such thing as an active high pass filter. Unlike Passive High Pass Filters which have an "infinite" frequency response, the maximum pass band frequency response of an active high pass filter is limited by the open-loop characteristics or bandwidth of the operational amplifier being used, making them appear as if they are band pass filters with a high frequency cut-off determined by the selection of op-amp and gain. In the Operational Amplifier tutorial we saw that the maximum frequency response of an op-amp is limited to the Gain/ Bandwidth product or open loop voltage gain (AV) of the operational amplifier being used giving it a bandwidth limitation, where the closed loop response of the op amp intersects the open loop response.

Second-order Active High Pass Filter Circuit



Higher-order high pass active filters, such as third, fourth, fifth, etc are formed simply by cascading together first and second-order filters. For example, a third order high pass filter is formed by cascading in series first and second order filters, a fourth-order high pass filter by cascading two second-order filters together and so on.

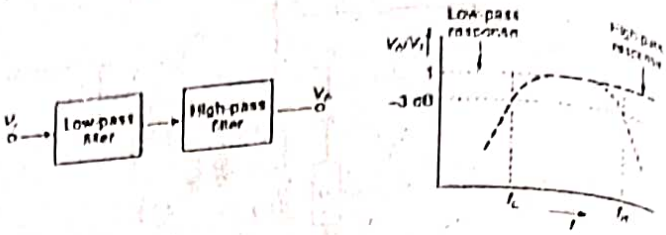
Q7. Explain Band pass filters using Operational Amplifier.

A *Band pass filters :* Filters that pass band of frequencies and attenuates others. Its high cutoff frequency and low cutoff frequency are related as fH >fL and maximum gain at resonant frequency

* fr= v fHfL
* Figure of merit Q= fr/ (fH- fL) = fr/B where B= bandwidth. 2 types of filters are Narrow band pass and wide band pass filters

Wide band pass filter :

* It is connection of a low pass filter and a high pass filter in cascade.
* The fH of low pass filter and fL of high pass filter are related as fH > fL



OBJECTIVE QUESTIONS AND ANSWERS

1. A differential amplifier .....
   1. is a part of an Op-amp
   2. has one input and one output
   3. has two outputs
   4. answers (1) and (2)

Ans : 4

2. When a differential amplifier is operated single-ended, ...
   1. the output is grounded
   2. one input is grounded and signal is applied to the other
   3. both inputs are connected together
   4. the output is not inverted

Ans : 2

3. In differential-mode, ...
   1. opposite polarity signals are applied to the inputs
   2. the gain is one
   3. the outputs are of different amplitudes
   4. only one supply voltage is used

Ans : 1

4. In the common mode, ...
   1. both inputs are grounded
   2. the outputs are connected together
   3. an identical signal appears on both the inputs
   4. the output signal are in-phase

Ans : 3

5. The common-mode gain is .....
   1. very high
   2. very low
   3. always unity
   4. unpredictable

Ans : 2

6. The differential gain is .....
   1. very high 2. very low
   3. dependent on input voltage
   4. about 100

Ans : 1

7. If ADM = 3500 and ACM = 0.35, the CMRR is .....
   1. 1225 2. 10,000
   3. 80 dB 4. answers (1) and (3)

Ans : 4

8. With zero volts on both inputs, an OP-amp ideally should have an output .....
   1. equal to the positive supply voltage
   2. equal to the negative supply voltage
   3. equal to zero
   4. equal to CMRR

Ans : 3

9. Of the values listed, the most realistic value for open-loop voltage gain of an OP-amp is .....
   1. 1 2. 2000
   3. 80 dB 4. 100,000

Ans : 4

10. A certain OP-amp has bias currents of 50 μA. The input offset current is .....
    1. 700 nA 2. 99.3 μA
    3. 49.7 μA 4. none of these

Ans : 1

11. The output of a particular Op-amp increases 8V in 12μs. The slew rate is .....
    1. 90 V/μs
    2. 0.67 V/μs
    3. 1.5 V/μs
    4. none of these

Ans : 2

12. For an Op-amp with negative feedback, the output is .....
    1. equal to the input
    2. increased
    3. fed back to the inverting input
    4. fed back to the noninverting input

Ans : 3

13. The use of negative feedback .....
    1. reduces the voltage gain of an Op-amp
    2. makes the Op-amp oscillate
    3. makes linear operation possible
    4. answers (1) and (2)

Ans : 4

14. Negative feedback .....
    1. increases the input and output impedances
    2. increases the input impedance and bandwidth
    3. decreases the output impedance and bandwidth
    4. does not affect impedance or bandwidth

Ans : 2

15. A certain noninverting amplifier has Ri of 1 kO and Rf of 100 kO. The closed-loop voltage gain is .....
    1. 100,000 2. 1000
    3. 101 4. 100

Ans : 3

16. If the feedback resistor in Q15 (above question) is open, the voltage gain .....
    1. increases 2. decreases
    3. is not affected 4. depends on Ri

Ans : 1

17. A certain inverting amplifier has a closed-loop voltage gain of 25. The Op-amp has an open-loop voltage gain of 100,000. If an Op-amp with an open-loop voltage gain of 200,000 is substituted in the arrangement, the closed-loop gain .....
    1. doubles
    2. drops to 12.5
    3. remains at 25
    4. increases slightly

Ans : 3

18. A voltage follower .....
    1. has a voltage gain of 1
    2. is noninverting
    3. has no feedback resistor
    4. has all of these

Ans : 4

19. The Op-amp can amplify
    1. a.c. signals only
    2. d.c. signals only

3. both a.c. and d.c. signals
4. neither d.c. nor a.c. signals

Ans : 3

20. The input offset current equals the .....
1. difference between two base currents
2. average of two base currents
3. collector current divided by current gain
4. none of these

Ans : 1

21. The tail current of a differential amplifier is .....
1. half of either collector current
2. equal to either collector current
3. two times either collector current
4. equal to the difference in base currents

Ans : 3

22. The node voltage at the top of the til resistor is closes to .....
1. collector supply voltage
2. zero
3. emitter supply voltage
4. tail current times base resistance

Ans : 2

23. The tail current in a differential amplifier equals .....
1. difference between two emitter currents
2. sum of two emitter currents
3. collector current divided by current gain
4. collector voltage divided by collector resistance

Ans : 2

24. The differential voltage gain of a differential amplifier is equal to RC divided by .....
1. r'e
2. r'e/2
3. 2r'e
4. RE

Ans : 3

25. The input impedance of a differential amplifier equals r'e times .....
1. ß
2. RE
3. RC
4. 2ß

Ans : 4

26. A common-mode signal is applied to .....
1. the noninverting input
2. the inverting input
3. both iputs
4. top of the tail resistor

Ans : 3

27. The common-mode voltage gain is .....
1. smaller than differentail voltage gain
2. equal to differential voltage gain
3. greater than differential voltage gain
4. none of the above

Ans : 1

28. The input stage of an Op-amp is usually a .....
1. differential amplifier
2. class B push-pull amplifier
3. CE amplifier
4. swamped amplifier

Ans : 1

29. The common-mode voltage gain of a differential amplifier is equal to RC divided by .....
1. r'e
2. 2r'e
3. r'e/2
4. 2RE

Ans : 4

30. Current cannot flow to ground through .....
1. a mechanical ground
2. an a.c. ground
3. a virtual ground
4. an ordinary ground

Ans : 3

UNIT 03

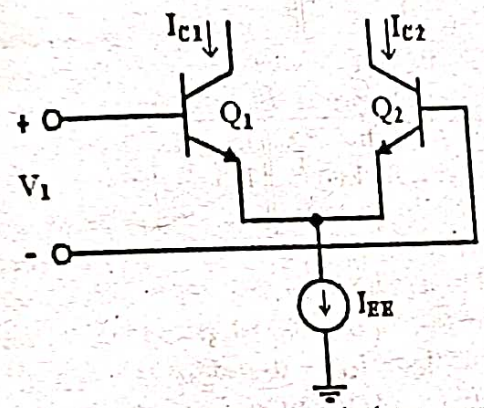
ANALOG MULTIPLIER AND PLL

QUESTIONS AND ANSWERS

Q1. Describe Analog multiplier using an Emitter coupled Transistor pair.

Ans. The output currents I_{C1} and I_{C2} are related to the differential input voltage V_1 by

$$I_{C1} = \frac{I_{EE}}{1+e^{V_1/V_T}} \text{ and } I_{C2} = \frac{I_{EE}}{1+e^{V_2/V_T}}$$



where V is thermal voltage and the base currents have been neglected. Combining above eqn., difference between the two output- currents as

$$\Delta I_C = I_{C1} - I_C$$

$$= \frac{I_{EE}}{1+e^{V_1/V_T}} - \frac{I_{EE}}{1+e^{V_2/V_T}}$$

$$= I_{EE} \tanh (V_1/2V_T)$$

The dc transfer characteristics of the emitter – coupled pair is shown in figure. It shows that the emitter coupled pair can be used as a simple multiplier using this configuration. When the differential input voltage V1 << VT, we can appropriate as given by

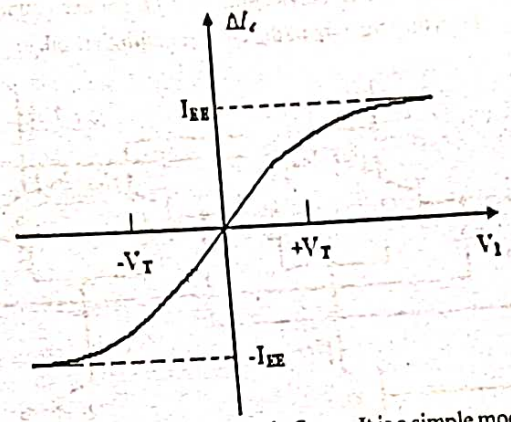
$$\delta I_C = I_{EE}(V1/2VT)$$

The current I_{EE} is the bias current for the emitter – coupled pair. If the current IEE is made proportional to a second input signal V_2, then

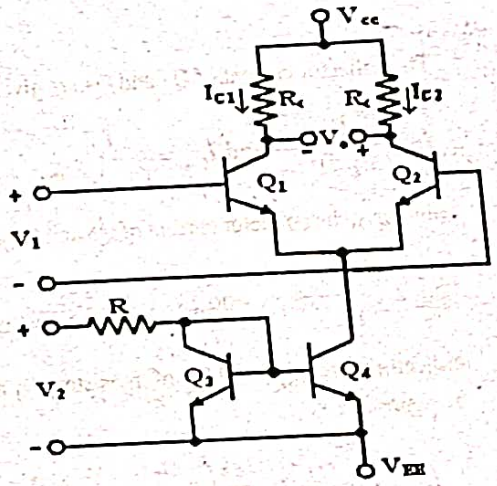
$$I_{EE} = K0 (V_2 - V_{BE})/2VT$$

Substituting above eqn. , we get

$$\delta IC = K0V_1 (V_2 - V_{BE})/2V_T$$



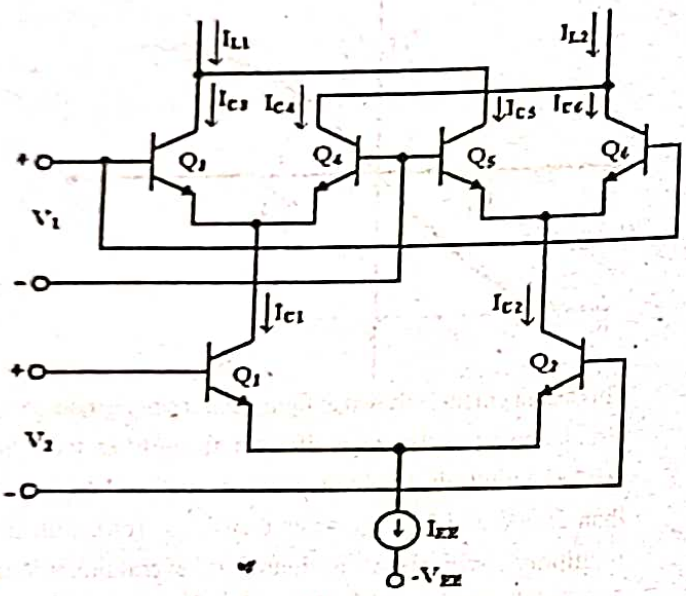
This arrangement is shown in figure. It is a simple modulator circuit constructed using a differential amplifier. It can be used as a multiplier, provided V1 is small and much less than 50mV and V2 is greater than V_{BE} (on). But, the multiplier circuit shown in figure has several limitations. The first limitation is that V2 is offset by V_{BE} (on).



The second is that V2 must always be positive which results in only a two-quadrant multiplier operation. The third limitation is that, the tanh (X) is approximately as X, where X = V_1 /2VT. The first two limitations are overcome in the Gilbert cell.

Q2. Explain Gilbert Multiplier cell.

Ans. The Gilbert multiplier cell is a modification of the emitter coupled cell and this allows four – quadrant multiplication. Therefore, it forms the basis of most of the integrated circuit balanced Multipliers. Two cross- coupled emitter- coupled pairs in series connection with an emitter coupled pair form the structure of the Gilbert multiplier cell.



The collector current of Q3 and Q4 are given by

$$I_{C3}\frac{I_{C1}}{1+e^{-V_1/V_T}} \text{ and } I_{C4}=\frac{I_{C1}}{1+e^{V_1/V_T}}$$

Similarly, the collector current of Q5 and Q6 are given by

$$\text{The } I_{C5}\frac{I_{C2}}{1+e^{V_1/V_T}} \text{ and } I_{C6}=\frac{I_{C2}}{1+e^{-V_1/V_T}}$$

collector current I_{C1} and I_{C2} of transistors Q_1 and Q_2 can be expressed as

$$I_{C1}=\frac{I_{EE}}{1+e^{-V_1/V_T}} \text{ and } I_{C2}=\frac{I_{EE}}{1+e^{V_2/V_T}}$$

Substituting the above equation in IC3 and IC4, we get

$$I_{C3}=\frac{I_{EE}}{\left[1+e^{\frac{-V_2}{V_t}}\right]\left[1+e^{-\frac{V_1}{V_T}}\right]}$$

$$I_{C4}=\frac{I_{EE}}{\left[1+e^{\frac{-V_2}{V_t}}\right]\left[1+e^{\frac{V_1}{V_T}}\right]}$$

and

Similarly substituting I_{c2}= in I_{c5} and I_{C6} , we get,.

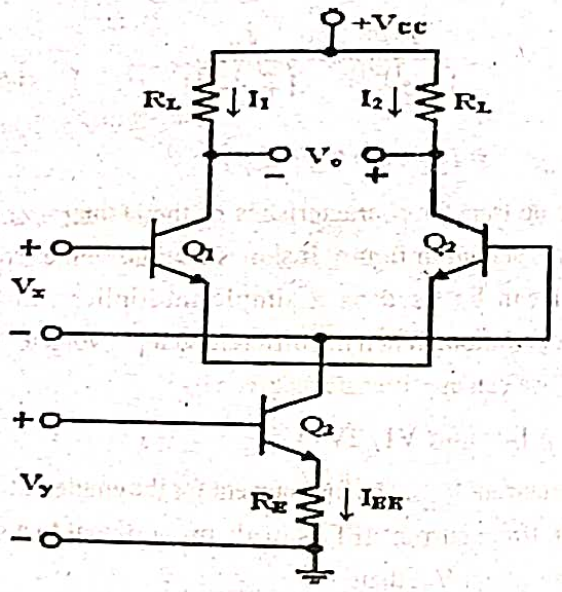
$$I_{C5}=\frac{I_{EE}}{\left[1+e^{\frac{V_2}{V_t}}\right]\left[1+e^{\frac{V_1}{V_T}}\right]}$$

$$\text{and } I_{C6}=\frac{I_{EE}}{\left[1+e^{\frac{V_2}{V_t}}\right]\left[1+e^{-\frac{V_1}{V_T}}\right]}$$

$$\delta I = I_{L1} - I_{L2}$$
$$= (I_{C3} + I_{C5}) - (I_{C4} + I_{C6})$$
$$= (I_{C3} - I_{C6}) - (I_{C4} - I_{C5})$$
$$\delta I = I_{EE} \tanh(V_1/2V_T) \tanh(V_2/2V_T).$$

Q3. Describe variable transconductance technique.

Ans



The variable transconductance technique makes use of the dependence characteristic of the transistor transconductance parameter on the emitter current bias applied. A simple differential circuit arrangement depicting the principle is shown in figure. The relationship between V_0 and Vx , is given by

$V_0 = gm\ R_L\ V_X$ where $gm = I_{EE}/V_T$ is the transconductance of the stage.

Application of a second input Vy to the reference current source of the differential amplifier can vary gm.

Thus, if $R_E I_{EE} >> V_{BE}$, the bias voltage Vy is related to I_{EE} by the relation $Vy = I_{EE} R_E$.

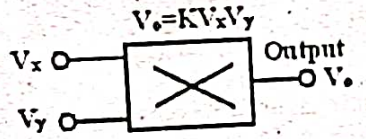
Then, the overall voltage transfer expression is given by

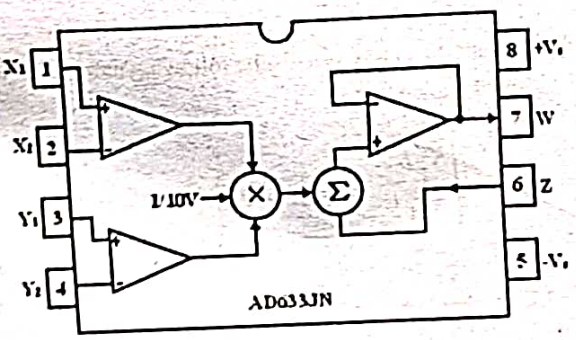
$$V_0 = g_m R_L Vx = (Vy/V_T R_E) Vx R_L$$
$$= VxVy\ R_L/V_T R_E$$

Q4. Explain Analog Multiplier ICs.

Ans. Analog multiplier is a circuit whose output voltage at any instant is proportional to the product of instantaneous value of two individual input voltages. Important applications of these multipliers are multiplication, division, squaring and square – rooting of signals, modulation and demodulation.

These analog multipliers are available as integrated circuits consisting of op-amps and other circuit elements. The Schematic of a typical analog multiplier, namely, AD633 is shown in figure.





- The AD633 multiplier is a four – quadrant analog multiplier.
- It possesses high input impedance; this characteristic makes the loading effect on the signal source negligible.
- It can operate with supply voltages ranging from ±18V.
- IC does not require external components.
- The typical range of the two input signals is ±10V.

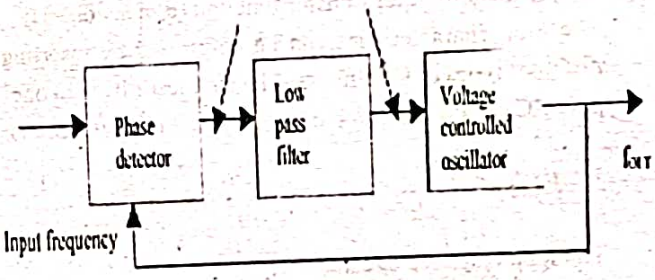
Schematic representation of a multiplier: The schematic representation of an analog multiplier is shown in figure. The output V0 is the product of the two inputs Vx and Vy is divided by a reference voltage Vref. Normally, the reference voltage Vref is internally set to 10V. Therefore, V0 = VxVy/10. In other words, the basic input – output relationship can be defined by KVx Vy when K = 1/10, a constant. Thus for peak input voltages of 10V, the peak magnitude of output voltage is 1/10 *10 *10 =10V. Thus, it can be noted that, as long as Vx < 10V and Vy < 10V, the multiplier output will not saturate.

Applications of Multiplier ICs: The multiplier ICs are used for the following purposes:

1. Voltage Squarer
2. Frequency doublers
3. Voltage divider
4. Square rooter
5. Phase angle detector
6. Rectifier

Q5. Explain Operation of Basic Phase Locked Loop (PLL).

Ans.



The PLL consists of

(i) Phase detector

(ii) LPF

(iii) VCO.

The phase detector or comparator compares the input frequency f_{IN} with feedback frequency f_{OUT}.

- The output of the phase detector is proportional to the phase difference between f_{IN} & f_{OUT}

The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage.

- The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces

a dc level. This dc level in turn, is input to the VCO.

- The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies.
- PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

Before the input is applied, the PLL is in free running state. Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode.

Q6. Describe Control System Analysis/ Closed Loop Analysis of PLL.

Ans. Phase locked loops can also be analyzed as control systems by applying the Laplace transform.

The loop response can be written as:

$$\frac{0_0}{\theta_i} = \frac{K_p K_v F(s)}{s + K_p K_v F(s)}$$

Where :

- θ_0 is the output phase in radians
- θ_i is the input phase in radians
- Kp is the phase detector gain in volts per radian
- Kv is the VCO gain in radians per volt-second
- F(s) is the loop filter transfer function (dimensionless)

The loop characteristics can be controlled by inserting different types of loop filters. The simplest filter is a one-pole RC circuit. The loop transfer function in this case is:

$$F(s) = \frac{1}{1 + sRC}$$

The loop response becomes:

$$\frac{\theta_0}{\theta_i} = \frac{\frac{K_p K_v}{RC}}{s^2 + \frac{s}{RC} + \frac{K_p K_v}{RC}}$$

This is the form of a classic harmonic oscillator. The denominator can be related to that of a second order system:

$$s^2 + 2s\zeta\omega_n + \omega_n^2$$

Where :

ζ is the damping factor

ωn is the natural frequency of the loop.

For the one-pole RC filter,

$$\omega_n = \sqrt{\frac{K_p K_v}{RC}}$$

$$\zeta = \frac{1}{2\sqrt{K_p K_v RC}}$$

The loop natural frequency is a measure of the response time of the loop, and the damping factor is a measure of the overshoot and ringing. Ideally, the natural frequency should be high and the damping factor should be near 0.707 (critical damping). With a single pole filter, it is not possible to control the loop frequency and damping factor independently. For the case of critical damping,

$$RC = \frac{1}{2K_p K_v}$$

$$\omega_c = K_p K_v \sqrt{2}$$

A slightly more effective filter, the lag-lead filter includes one pole and one zero. This can be realized with two resistors and one capacitor. The transfer function for this filter is

$$F(s) = \frac{1 + sCR_2}{1 + sC(R_1 + R_2)}$$

This filter has two time constants :

$t_1 = C(R_1 + R_2)\, t_2$

$= CR_2$

Substituting above yields the following natural frequency and damping factor

$$\omega_n = \sqrt{\frac{K_p K_v}{\tau_1}}$$

$$\zeta = \frac{1}{2\omega_n \tau_1} + \frac{\omega_n \tau_2}{2}$$

The loop filter components can be calculated independently for a given natural frequency and damping factor

$$\tau_1 = \frac{K_p K_v}{\omega_n^2}$$

$$\tau_2 = \frac{2\zeta}{\omega_n} - \frac{1}{K_p K_v}$$

Real world loop filter design can be much more complex eg using higher order filters to reduce various types or source of phase noise.

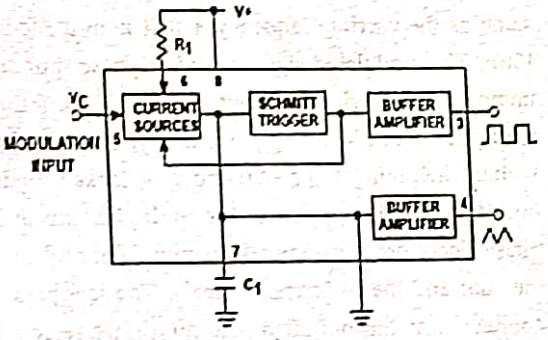
Applications of PLL:

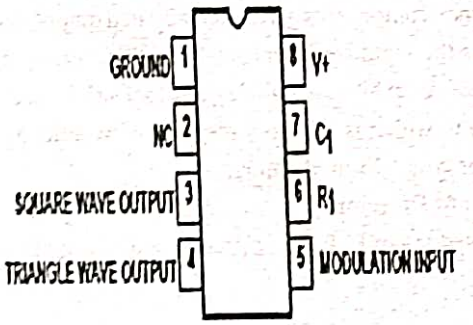
The PLL principle has been used in applications such as :

- FM stereo decoders
- Motor speed control
- Tracking filters
- FM modulation and demodulation
- FSK modulation
- Frequency multiplier
- Frequency synthesis etc.,

Q7. Define Voltage Controlled Oscillator.

Ans.





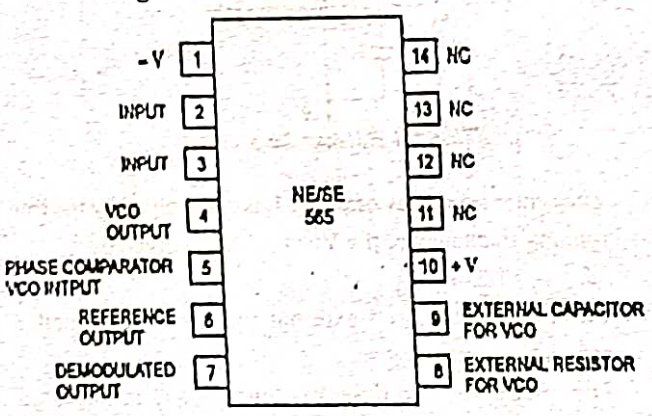
Referring to the circuit in the above figure, the capacitor c1 is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage vc applied at the modulating input (pin 5) or by changing the timing resistor R1 external to the IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R1 and thereby decreasing the charging current. The voltage across the capacitor C1 is applied to the inverting input terminal of Schmitt trigger via buffer amplifier. The output voltage swing of the Schmitt trigger is designed to Vcc and 1.5 Vcc. If Ra = Rb in the positive feedback loop, the voltage at the non-inverting input terminal of Schmitt trigger swings from 0.5 Vcc to 0.25 Vcc.When the voltage on the capacitor c1 exceeds 0.5 Vcc during charging, the output of the Schmitt trigger goes LOW (0.5 Vcc). The capacitor now discharges and when it is at 0.25 Vcc, the output of Schmitt trigger goes HIGH (Vcc). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across c1 which is also available at pin 4.The square wave output of the Schmitt trigger is inverted by buffer amplifier at pin 3. The output waveforms are shown near the pins 4 and 3.The output frequency of the VCO can be given as follows:

$$f_0 = \frac{2[(V+)-(V_C)]}{R_1 C_1 V+}$$

where V+ is Vcc.

Q8. Describe Monolithic Phase Locked Loops (PLL IC 565).

Ans. Pin Configuration of PLL IC 565

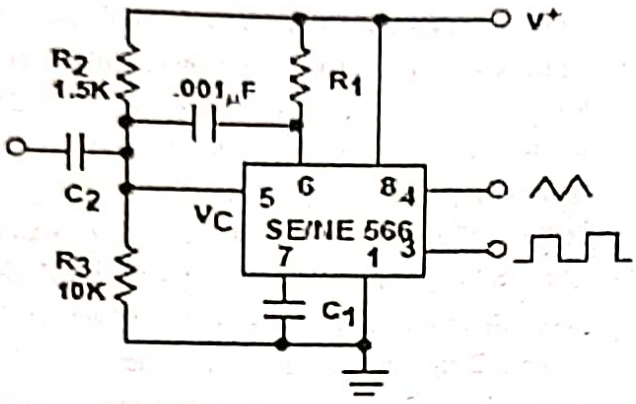


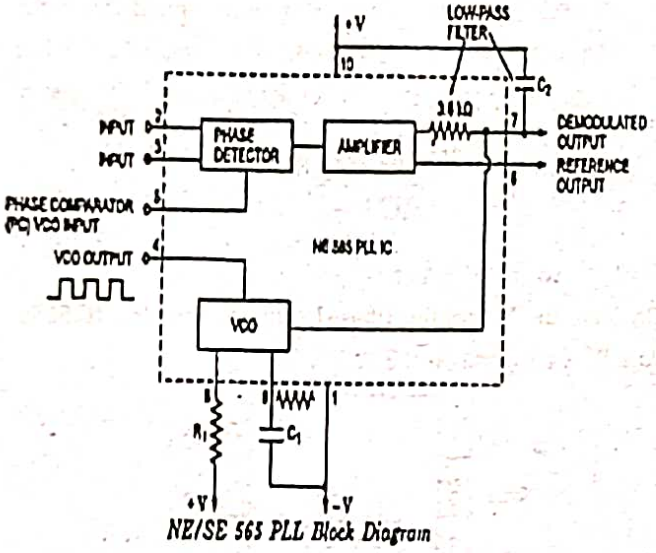
14-Pin DIP Package

Basic Block Diagram Representation of IC 565

The important electrical characteristics of the 565 PLL are,

- Operating frequency range: 0.001Hz to 500 Khz.
- Operating voltage range: ±6 to ±12v
- Input level required for tracking: 10mv rms min to 3 Vpp max
- Input impedance: 10 K ohms typically.
- Output sink current: 1mA
- Output source current: 10 Ma





NE/SE 565 PLL Block Diagram

The center frequency of the PLL is determined by the free running frequency of the VCO, which is given by

$f_{OUT} = 1.2/4R_1C_1$

where R1&C1 are an external resistor & a capacitor connected to pins 8 & 9.

- The VCO free-running frequency f_{OUT} is adjusted externally with R_1 & C_1 to be at the center of the input frequency range.
- C1 can be any value; R_1 must have a value between 2 k ohms and 20 K ohms.
- Capacitor C_2 connected between 7 & +V.
- The filter capacitor C_2 should be large enough to eliminate variations in the demodulated output voltage in order to stabilize the VCO frequency.

The lock range fL & capture range fc of PLL is given by,

$$\delta f_L = \pm 7.8 \text{ fout / V Hz}$$

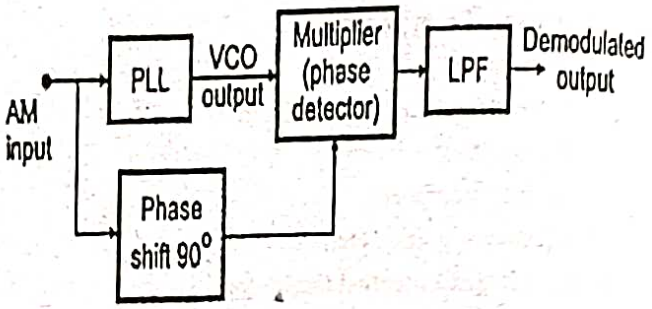
Where f_{OUT} = free running frequency of VCO (Hz)

V = (+Vcc) – (–Vcc) volts

$$\delta f_C = \pm [\delta f_L / (2\delta)(3.6)(10^3)C_2]^{1/2}$$

Q9. Explain AM Detection using PLL.

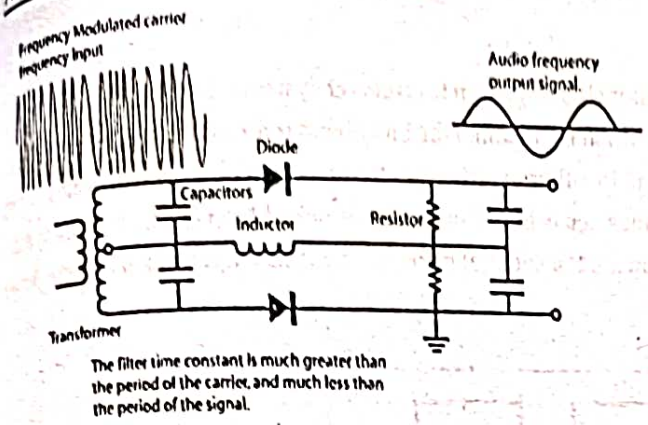
Ans. AM Detection – A PLL can be used to demodulate AM signals as shown in the Fig.



The PLL is locked to the carrier frequency of the incoming AM signal. Once locked the output frequency of VCO is same as the carrier frequency, but it is in unmodulated form. The modulated signal with 90° phase shift and the unmodulated carrier from output of PLL are fed to the multiplier. Since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, both the signals applied to the multiplier are in same phase. Therefore, the output of the multiplier contains both the sum and the difference signals. The low pass filter connected at the output of the multiplier rejects high frequency components gives demodulated output. As PLL follows the input frequencies with high accuracy, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

Q10. Define FM Detector

The detection of FM radio signals is a diode application.



Q11. Explain FSK modulation and demodulation.

Ans. ***FSK Modulator :*** The FSK modulator block diagram comprises of two oscillators with a clock and the input binary sequence. Following is its block diagram.

FSK Transmitter

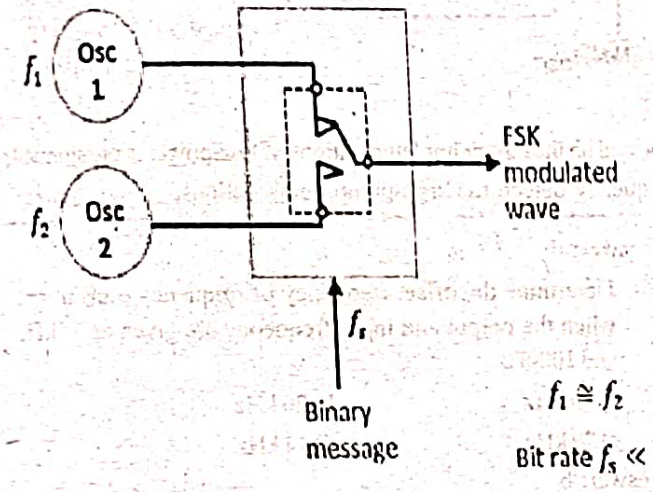
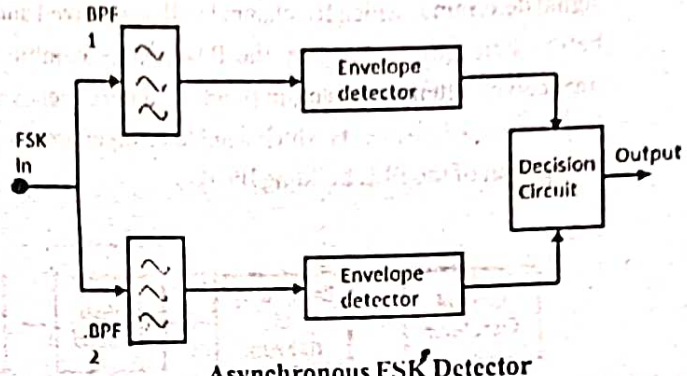


Fig. FSK Transmitter

The two oscillators, producing a higher and a lower frequency signals, are connected to a switch along with an internal clock. To avoid the abrupt phase discontinuities of the output waveform during the transmission of the message, a clock is applied to both the oscillators, internally. The binary input sequence is applied to the transmitter so as to choose the frequencies according to the binary input.

FSK Demodulator : There are different methods for demodulating a FSK wave. The main methods of FSK detection are synchronous detector and synchronous detector. The synchronous detector is a coherent one, while asynchronous detector is a non-coherent one.

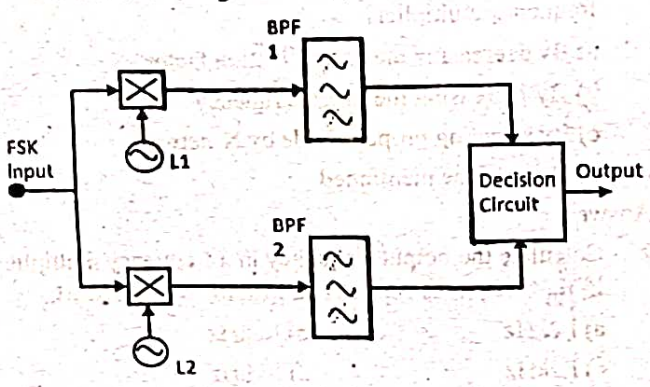
Asynchronous FSK Detector : The block diagram of Asynchronous FSK detector consists of two band pass filters, two envelope detectors, and a decision circuit. Following is the diagrammatic representation.



Asynchronous FSK Detector

The FSK signal is passed through the two Band Pass Filters BPFs, tuned to Space and Mark frequencies. The output from these two BPFs look like ASK signal, which is given to the envelope detector. The signal in each envelope detector is modulated asynchronously. The decision circuit chooses which output is more likely and selects it from any one of the envelope detectors. It also re-shapes the waveform to a rectangular one.

Synchronous FSK Detector : The block diagram of Synchronous FSK detector consists of two mixers with local oscillator circuits, two band pass filters and a decision circuit. Following is the diagrammatic representation.



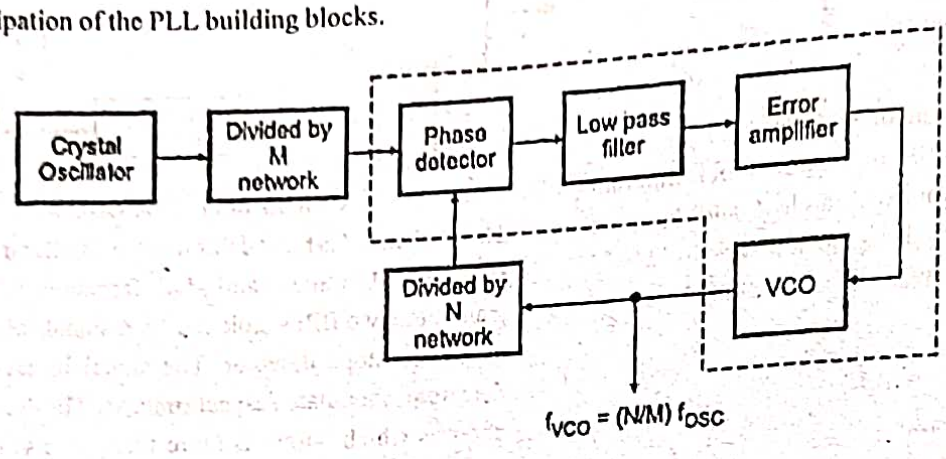
Synchronous FSK Detector

The FSK signal input is given to the two mixers with local oscillator circuits. These two are connected to two band pass filters. These combinations act as demodulators and the decision circuit chooses which output is more likely and selects it from any one of the detectors. The two signals have a minimum frequency separation. For both of the demodulators, the bandwidth of each of them depends on their bit rate. This synchronous demodulator is a bit

complex than asynchronous type demodulators.

Q12. Explain Frequency Synthesizers.

Ans. Frequency synthesizers are used to generate the local oscillator (LO) signal in transceiver systems. The frequency of the LO signal determines which RF channel will be received and to which RF channel the base-band information will be transferred before being transmitted by the PA-antenna combination. In other words, the frequency synthesizer operates as the transceiver's tuning system; in practice, the frequency synthesizer is based on a phase-locked loop (PLL) control system. Important design aspects which need to be taken into account are the spectral purity of the PLL output signal and the power dissipation of the PLL building blocks.



The spectral purity performance of PLL frequency synthesizers, and on the circuit implementations of low-power programmable frequency dividers and high operation frequency phase-frequency detector/charge-pump combinations.

OBJECTIVE QUESTIONS AND ANSWERS

1. How to obtain a desired amount of multiplication in frequency multiplier?
   a) By decreasing the multiplication factor
   b) By increasing the input frequency
   c) By selecting proper divide by N-network
   d) None of the mentioned

Answer: c

2. Calculate the output frequency in a frequency multiplier if, f_{in} = 200Hz is applied to a 7 divide by N-network.
   a) 1.2kHz b) 1.6kHz
   c) 1.2kHz d) 1.9kHz

Answer: c

3. For what kind of input signal, the frequency divider can be avoided frequency multiplier?
   a) Triangular waveform b) Square waveform
   c) Saw tooth waveform d) Sine waveform

Answer: a

4. What must the typical value of n for a frequency multiplication / division? (n->order of harmonics)
   a) n d" 12 b) n > 11
   c) n < 10 d) n = 7

Answer: d

5. Determine the offset frequency of frequency translation, when the output and input frequency are given as 75kHz and 1000Hz.
   a) 35 kHz b) 20 kHz
   c) 29 kHz d) 14 kHz

Answer: b

6. The frequency corresponding to logic 1 state in FSK is called
   a) Space frequency b) Mark frequency
   c) Both mark and space frequency
   d) None of the mentioned

Answer: b

7. Find the frequency shift in FSK generator?
   a) 230 Hz b) 250 Hz
   c) 180 Hz d) 200 Hz

Answer: d

8. Which filter is chosen to remove the carrier component in the frequency shift keying?
   a) Three stage filter b) Two stage filter
   c) Single stage filter d) All of the mentioned

Answer: a

9. Calculate the output frequency in a frequency multiplier if, $f_{in} = 200Hz$ is applied to a 7 divide by N-network.
   a) 1.2kHz b) 1.6kHz
   c) 1.2kHz d) 1.9kHz

Answer : c)

10. For what kind of input signal, the frequency divider can be avoided frequency multiplier?
   a) Triangular waveform
   b) Square waveform
   c) Saw tooth waveform
   d) Sine waveform

Answer : a)

11. How to obtain a desired amount of multiplication in frequency multiplier?
   a) By decreasing the multiplication factor
   b) By increasing the input frequency
   c) By selecting proper divide by N-network
   d) None of the mentioned

Answer : c)

12. What must the typical value of n for a frequency multiplication / division? (n->order of harmonics)
   a) $n \leq 12$ b) $n > 11$
   c) $n < 10$ d) $n = 7$

Answer : d)

13. The frequency corresponding to logic 1 state in FSK is called
   a) Space frequency b) Mark frequency
   c) Both mark and space frequency
   d) None of the mentioned

Answer : b)

14. Which filter is chosen to remove the carrier component in the frequency shift keying?
   a) Three stage filter b) Two stage filter
   c) Single stage filter d) All of the mentioned

Answer : a)

15. Determine the offset frequency of frequency translation, when the output and input frequency are given as 75kHz and 1000Hz.
   a) 35 kHz b) 20 kHz
   c) 29 kHz d) 14 kHz

Answer : b)

16. Find the frequency shift in FSK generator?
   a) 230 Hz b) 250 Hz
   c) 180 Hz d) 200 Hz

Answer : d)

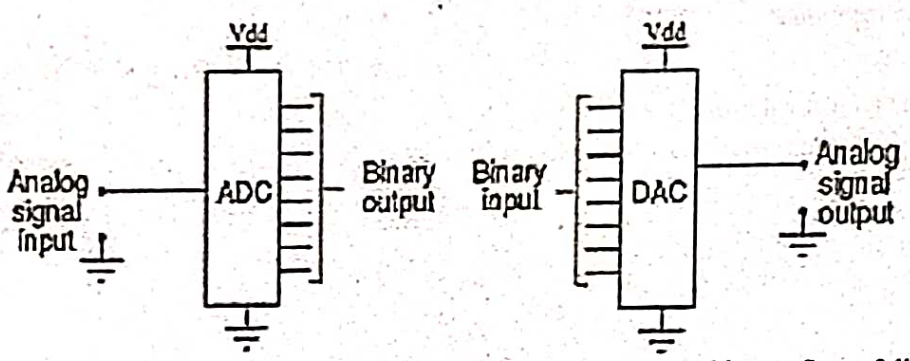
UNIT 04

ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS

QUESTIONS AND ANSWERS

Q1. Describe Analog and Digital Data Conversions.

Ans. Analog To Digital Conversion : The natural state of audio and video signals is analog. When digital technology was not yet around, they are recorded or played back in analog devices like vinyl discs and cassette tapes. The storage capacity of these devices is limited and doing multiple runs of re-recording and editing produced poor signal quality. Developments in digital technology like the CD, DVD, Blu-ray, flash devices and other memory devices addressed these problems.For these devices to be used, the analog signals are first converted to digital signals using analog to digital conversion (ADC). For the recorded audio and video signals to be heard and viewed again, the reverse process of digital to analog conversion (DAC) is used.ADC and DAC are also used in interfacing digital circuits to analog systems.



- Sampling rate : The analog signal is continuous in time and it is necessary to convert this to a flow of digital values. It is therefore required to define the rate at which new digital values are sampled from the analog signal.
- Accuracy : An ADC has several sources of errors. Quantization error and (assuming the ADC is intended to be linear) non-linearity is intrinsic to any analog-to-digital conversion. There is also a so-called aperture error which is due to a clock jitter and is revealed when digitizing a time-variant signal (not a constant value).
- Quantization error : Quantization error is due to the finite resolution of the ADC, and is an unavoidable imperfection in all types of ADC. The magnitude of the quantization error at the sampling instant is between zero and half of one LSB.At lower levels the quantizing error becomes dependent of the input signal, resulting in distortion.
- Non-linearity : All ADCs suffer from non-linearity errors caused by their physical imperfections, resulting in their output to deviate from a linear function (or some other function, in the case of a deliberately non-linear ADC) of their input. These errors can sometimes be mitigated by calibration, or prevented by testing.

D To A Converter- Specifications : D/A converters are available with wide range of specifications specified by manufacturer. Some of the important specifications are Resolution, Accuracy, linearity, monotonicity, conversion time, settling time and stability.

- Resolution : Resolution is defined as the number of different analog output voltage levels that can be provided by a DAC. Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input. Simply, resolution is the value of LSB.

Resolution (Volts) = VoFS / (2n – 1) = 1 LSB increment Where 'n' is the number of input bits 'VoFS' is the full scale output voltage.

* **Accuracy :** Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. The ideal converter is the one which does not suffer from any problem. Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors.

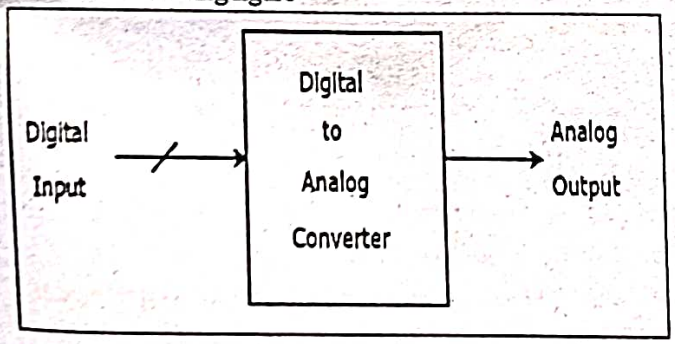
* **Linearity :** Linearity error is the maximum deviation in step size from the ideal step size. Some D/A converters are having a linearity error as low as 0.001% of full scale.

* **Monotonicity :** A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. A monotonic characteristic is essential in control applications. Otherwise it would lead to oscillations. If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. Hence all the D/A converters are designed such that the linearity error satisfies the above condition.

* **Conversion Time :** It is the time taken for the D/A converter to produce the analog output for the given binary input signal. It depends on the response time of switches and the output of the Amplifier. D/A converters speed can be defined by this parameter. It is also called as setting time.

Q2. Define Digital to Analog Converters.

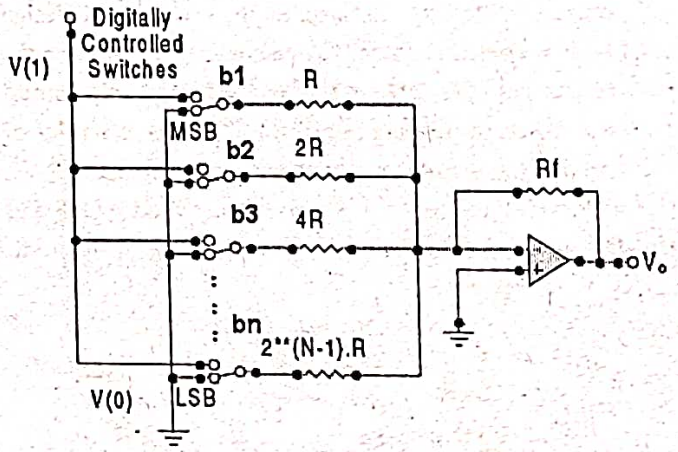
Ans. A Digital to Analog Converter (DAC) converts a digital input signal into an analog output signal. The digital signal is represented with a binary code, which is a combination of bits 0 and 1. This chapter deals with Digital to Analog Converters in detail.The block diagram of DAC is shown in the following figure -



A Digital to Analog Converter (DAC) consists of a number of binary inputs and a single output. In general, the number of binary inputs of a DAC will be a power of two.

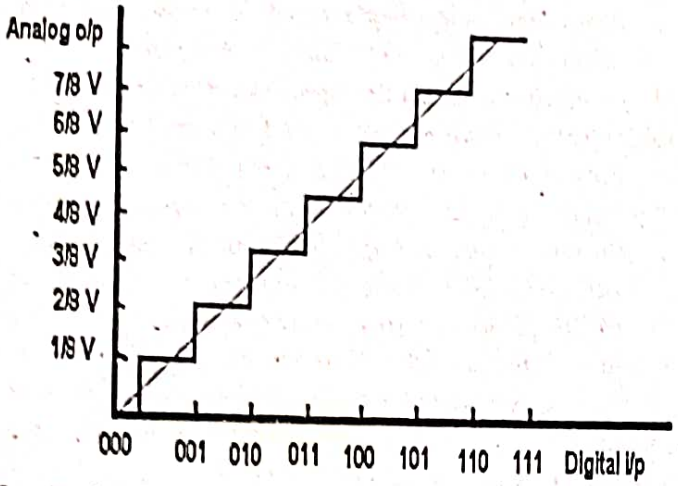
Q3. Weighted resistor for the digital to analog Converter.

Ans. Weighted resistor of digital to analog Converter is a very basic D/A converter. By using simple resistor network we can easily build that. As we discuss earlier about how digital to analog converters works you may refer that first. Let us consider a N-bit straight binary resistor network, which produces a current I corresponding to logic 1 at the most significant bit, I/2 corresponding to logic 1 at the next lower bit, I/22 for the next lower bit and so on, and I/ 2N–1 for logic 1 at the least significant bit position. Now the total current thus produced by that resistive network will be proportional to the digital inputs, which we want to convert in equivalent analog signal. Farther this current can be converted to voltage with the help of a converter circuit by an using operational amplifier (OP AMP). Finally then we get the produced voltage is analog in nature and will be proportional to the digital inputs. Now see the circuit bellow



It may be observed in the circuit diagram that different values of resistances are used at the digital inputs and the resistance values are the multiple of the resistance corresponding to the most significant digital input to produce the currents I, I/2, I/22, ... I/ 2N–1. Since the resistance values are weighted in accordance with the binary weights of the digital inputs, this circuit is referred to as a weighted-resistor D/A converter..

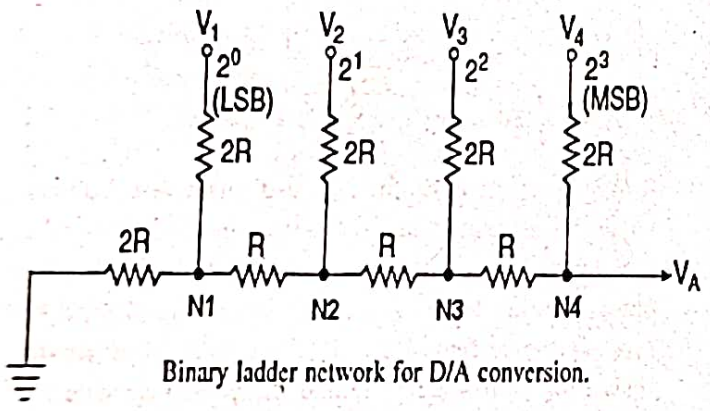
Diagram of weighted resistor digital to analog converter



Q4. Explain R-2R ladder D/A converter and its uses.

Ans. To overcome huge range of resistor used in weighted resistor D/A converter, R-2R ladder D/A converter is introduced. In my previous post I discussed about weighted resistor D/A conver.er.

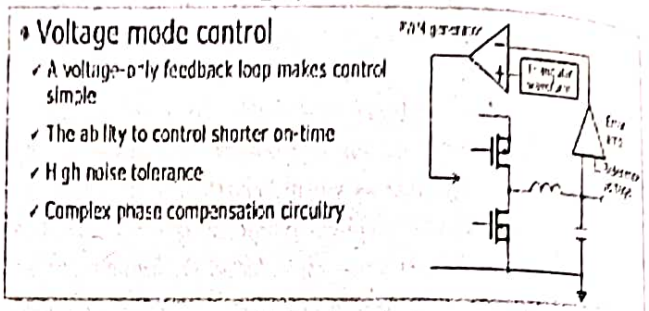
Use of R-2R ladder D/A converter : As we know the vital problem in weighted register D/A converter is use of huge range of different resistance. Suppose we have to design 8-bit weighted register D/A converter then we need the resistance value 20R + 21R +....+ 27R. So the largest resistor corresponding to bit b8 is 128 times the value of the smallest resistor correspond to b1. But in case of R-2R ladder D/A converter, Resistors of only two value (R and 2R) are used. Now in bellow see the simple ladder network.



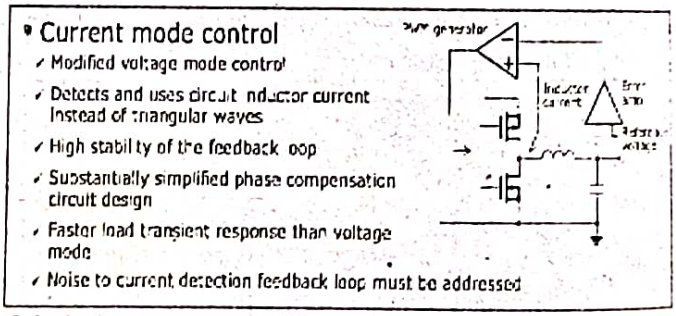
Binary ladder network for D/A conversion.

Q5. Explain Voltage Mode and Current-Mode.

Ans. *Voltage mode :* Voltage mode control represents the most basic method, in which only the output voltage is returned through a feedback loop. The differential voltage, which is obtained to compare the output voltage with the reference voltage by an error amp, is compared with triangular waves by a PWM generator. As a result, the pulse width of the PWM signal is determined to control the output voltage. Advantages of this method are its relative simplicity based on the use of a feedback loop consisting solely of voltages, the ability to control shorter on-time, and high noise tolerance. Possible drawbacks are the complexity of the phase compensation circuit and a cumbersome design process.



Current mode : The current mode is a modification of voltage mode control, where the inductor current in the circuit is detected and used instead of the triangular waveforms used in the voltage mode control. The current sensing can also be done by using the on-resistance of high side MOSFET or a current sense resistor instead of the inductor current. Since the current mode has two types of feedback loops: voltage loop and current loop, the control exerted is relatively complex. However the current mode provides the advantage of a substantially simplified phase compensation circuit design. Other benefits include the highly stable feedback loop and a faster load transient response than that of the voltage mode. A drawback is low-noise tolerance due to the high sensitivity of current detection. In the newer designs, however, the current detection part is built into the IC to alleviate the problem.



Q6. Switches for D/A converters.

Ans. The Switches which connects the digital binary input to the nodes of a D/A converter is an electronic switch. Although switches can be made of using diodes, bipolar

junction Transistors, Field Effect transistors or MOSFETs, there are four main configurations used as switches for DACs. They are :

(i) Switches using overdriven Emitter Followers.

(ii) Switches using MOS Transistor- Totem pole MOSFET Switch and CMOS Inverter Switch.

(iii) CMOS switch for Multiplying type DACs.

(iv) CMOS Transmission gate switches.

These configurations are used to ensure the high speed switching operations for different types of DACs.

1. **Switches using overdriven Emitter Followers :** The bipolar transistors have a negligible resistance when they are operated in saturation. The bipolar transistor operating in saturation region indicates a minimum resistance and thus represents ON condition. When they are operating in cut-off region indicates a maximum resistance and thus represents OFF condition.
2. **Switches using MOS transistor:**

(i) **Totem pole MOSFET Switch :** As shown in the figure, the totem pole MOSFET Switch is connected in series with resistors of R–2R network. The MOSFET driver is connected to the inverting terminal of the summing op-amp.

(ii) **CMOS Inverter Switch :** The figure of CMOS inverter is shown here. It consists of a CMOS inverter connected with an op-amp acting as a buffer. The buffer drives the resistor R with very low output impedance.

3. **CMOS switch for Multiplying type DACs :** The circuit diagram of CMOS Switch is shown here. The heart of the switching element is formed by transistors M1 and M2. The remaining transistors accept TTL or CMOS compatible logic inputs and provides the anti-phase gate drives for the transistors M1 and M2.
4. **CMOS Transmission gate switches :** The disadvantage of using individual NMOS and PMOS transistors are threshold voltage drop (NMOS transistor passing only minimum voltage of VR- VTH and PMOS transistor passing minimum voltage of VTH). This is eliminated by using transmission gates which uses a parallel connection of both NMOS and PMOS. The arrangement shown here can pass voltages from VR to 0V acting as a ideal switch. The following cases explain the operation.

Q7. Describe high speed sample-and-hold circuits.

Ans. Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing. Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits . The simplest S/H circuit in MOS technology is shown in Fig. 1, where V_{in} is the input signal, M1 is an MOS transistor operating as the sampling switch, Ch is the hold capacitor, ck is the clock signal, and Vout is the resulting sample-and-hold output signal. As depicted by Fig.4. , in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward.

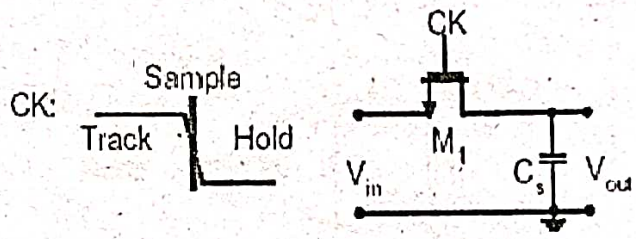


Fig. in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever ck is high, the MOS switch is on, which in turn allows Vout to track Vin. On the other hand, when ck is low, the MOS switch is off. During this time, Ch will keep Vout equal to the value of Vin at the instance when ck goes low. Unfortunately, in reality, the performance of this S/H circuit is not as ideal as described above. The two major types of errors occur. They are charge injection and clock feed through, that are associated with this S/H implementation. Three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through.

Q8. Describe Flash A/D Converters.

Ans. Flash ADCs are fast and operate virtually without latency, which is why they are the architecture of choice when the highest possible sample rates are needed. They convert analog to a digital signal by comparing it with known reference values. The more known references that are used in the conversion process, the more accuracy can be achieved. For example, if we want a Flash ADC with a 10-bit resolution, we would need to compare the incoming analog signal against 1024 known values. The 8-bit

resolution would require 256 known values, and so on. The more resolution we want, the bigger and more power-hungry the Flash ADC becomes - and the sample rate has to be reduced. For that reason, the 8-bit resolution is generally the "sweet spot" for these ADCs. Flash ADCs can operate into the low GS/s and still provide an 8-bit resolution.

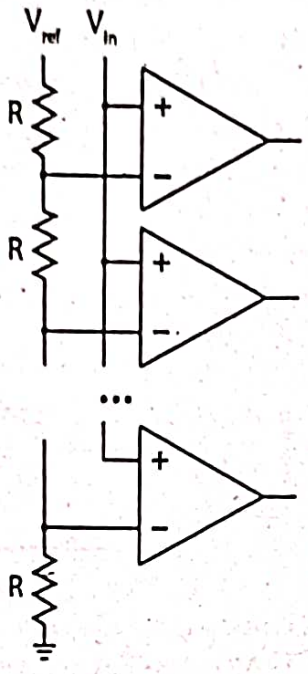
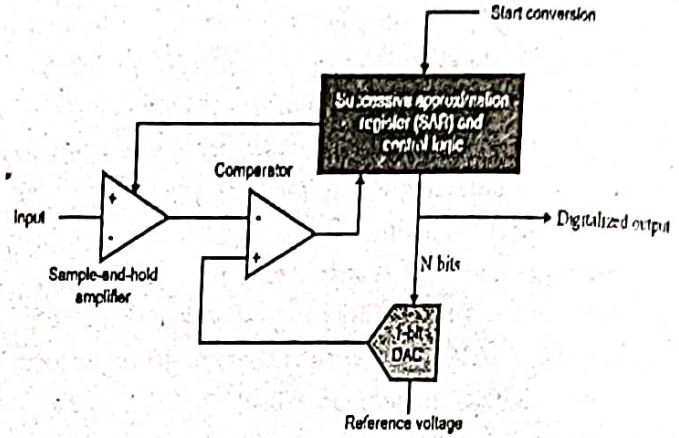


Fig. Flash ADC diagram

Q9. Successive Approximation ADCs (SAR). ?

Ans. The "bread and butter" ADC of the DAQ world is the SAR analog-to-digital converter (Successive Approximation Register). It offers an excellent balance of speed and resolution and handles a wide variety of signals with excellent fidelity. It's been around for a long time, therefore SAR designs are stable and reliable, and the chips are relatively inexpensive. They can be configured for both low-end A/D cards, where a single ADC chip is "shared" by multiple input channels (multiplexed A/D boards), or in configurations where each input channel has its own ADC for true simultaneous sampling.

The analog input of most ADCs is 5V, which is why nearly all signal conditioning front-ends provide a conditioned output that is the same. The typical SAR ADC uses a sample-and-hold circuit that takes in the conditioned analog voltage from the signal conditioning front-end. An on-board DAC creates an analog reference voltage equal to the digital code output of the sample and holds a circuit.

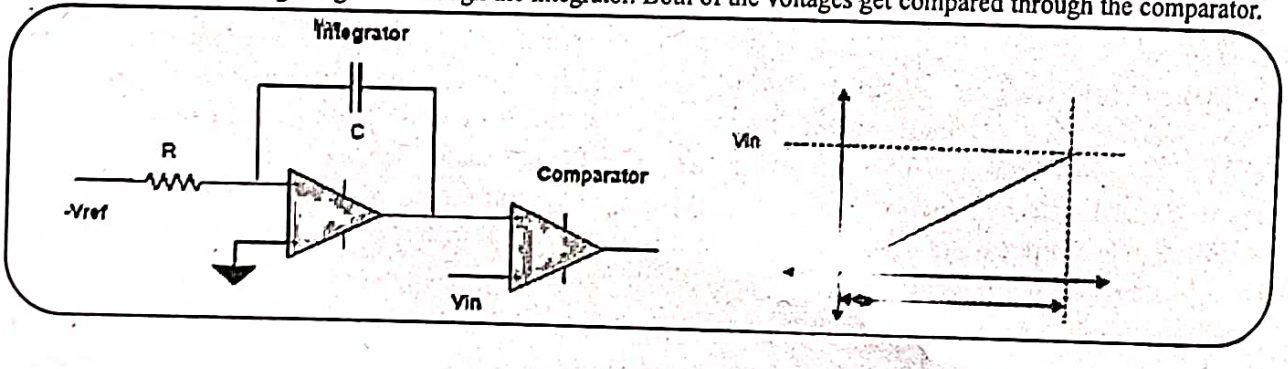


Typical SAR block diagram

Both of these are fed into a comparator which sends the result of the comparison to the SAR. This process continues for "n" successive times, with "n" being the bit resolution of the ADC itself, until the closest value to the actual signal is found. SAR ADCs do not have any inherent anti-aliasing filtering (AAF), so unless this is added before the ADC by the DAQ system, if the engineer selects too low of a sample rate, false signals (aka "aliases") will be digitized by the SAR ADC. Aliasing is particularly problematic because it is impossible to correct it after digitization.

Q10. Define Single slope ADC (Integrated ADC) and draw its ckt diagram.

Ans. Single slope adc circuit : The input voltage is applied to the positive terminal of the comparator while the reference voltage is obtained after being integrated through the integrator. Both of the voltages get compared through the comparator.



The input voltage is a function of time t. The reference voltage keeps on integrated until the output voltage of the comparator becomes equal to the input voltage.

The general output voltage of the integrator is given as

$$VO = 1/RC\,(-V_{ref})\,dt$$

In the equation, we can see that the reference voltage is negative, so the slope of the integrated output voltage turns out to be positive.

The output voltage of the integrator at any given time is given as

$$VO = T*V_{ref}\ /RC$$

At time T, the output voltage is equivalent to the input voltage. So, we can say

$$V_{in} = T*V_{ref}\ /RC$$

As the reference voltage, resistor R, and capacitor C are fixed for a given analog to digital converter, the input voltage is directly proportional to time.

Schematic diagram

Below is the schematic diagram of a single slope analog to digital converter:

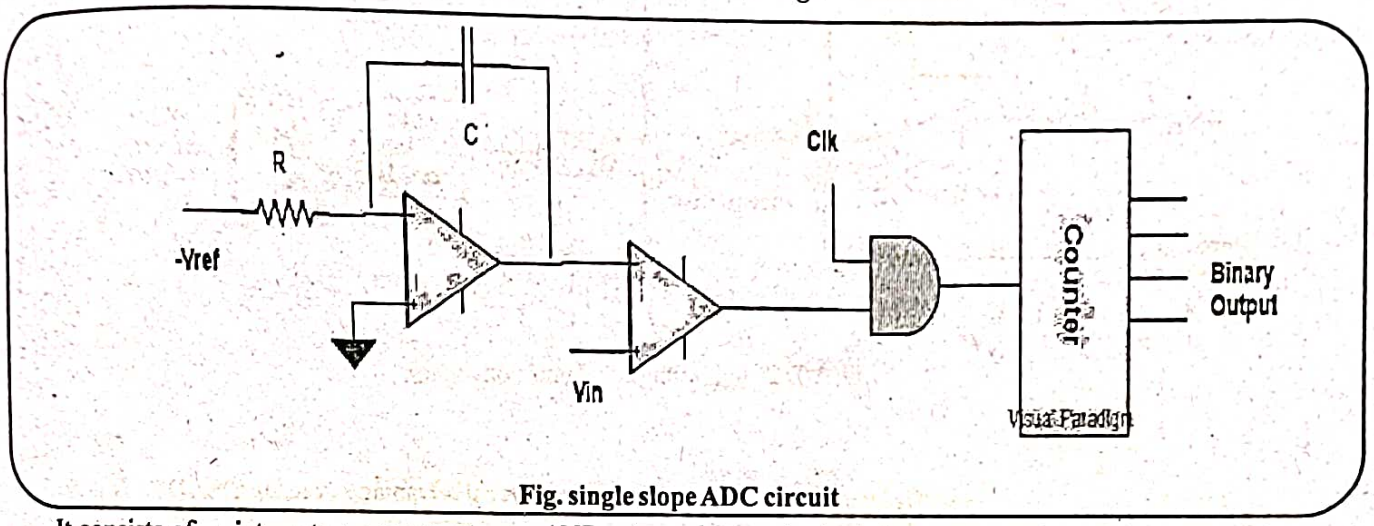
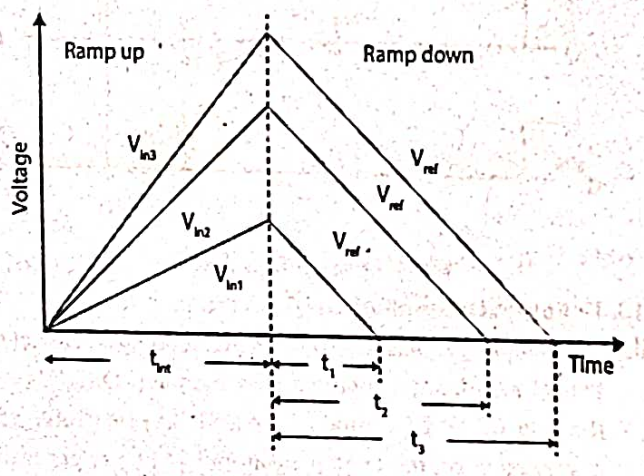


Fig. single slope ADC circuit

It consists of an integrator, a comparator, an AND gate, and a counter that gives us the binary outputs. The output of the comparator is passed to the AND gate. Whenever the output of the comparator is high which means that when the reference voltage is lesser than the input voltage, clock pulses are given to the counter through the AND gate, and the counter starts counting.

Q11. Explain Dual Slope A/D Converters.

Ans. Dual slope ADCs are accurate but not terribly fast. The principle way they convert analog to digital values is by using an integrator. The voltage is input and allowed to "run up" for a period of time. Then a known voltage of the opposite polarity is applied and allowed to run back down to zero. When it reaches zero, the system calculates what the input voltage had been by comparing the run-up time with the run-down time, and by knowing what the reference had been. The run-up and run-down times are the two slopes for which this technique has been named.This iterative process is reliable, but it takes time, and there is always a trade-off between resolution and speed because unlike SAR or delta-sigma ADCs, they cannot achieve both. As a result, Dual Slope aka "integrating ADCs" are used in applications like handheld multimeters and are not found in DAQ applications.



Typical Integrating Amplifier, showing the comparator, timer, and controller

Q12. Describe A/D Using Voltage To Time Conversion.

Ans. The Block diagram shows the basic voltage to time

conversion type of A to D converter. Here the cycles of variable frequency source are counted for a fixed period. It is possible to make an A/D converter by counting the cycles of a fixed-frequency source for a variable period. For this, the analog voltage required to be converted to a proportional time period.

As shown in the diagram a negative reference voltage -VR is applied to an integrator, whose output is connected to the inverting input of the comparator. The output of the comparator is at 1 as long as the output of the integrator Vo is less than Va.

At $t = T$, Vc goes low and switch S remains open. When VEN goes high, the switch S is closed, thereby discharging the capacitor. Also the NAND gate is disabled. The waveforms are shown here.

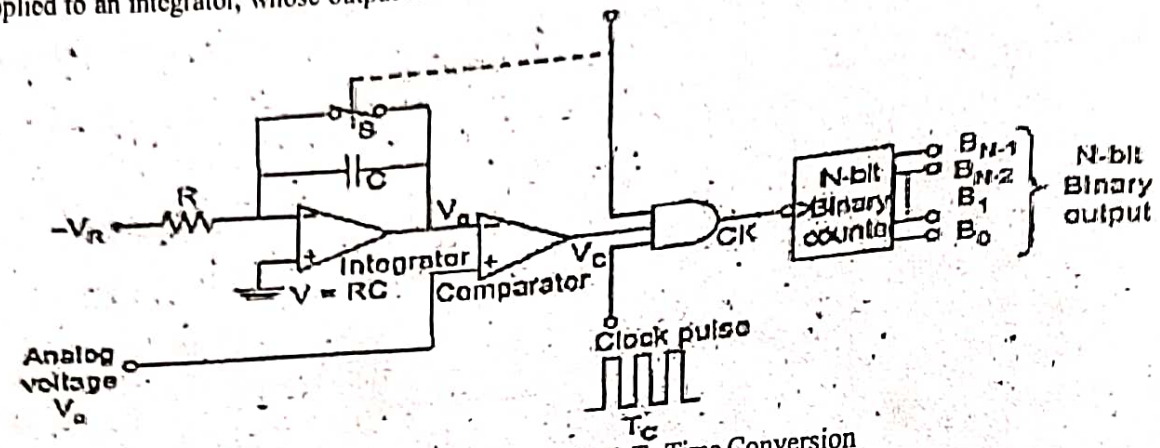


Fig. A/D Using Voltage To Time Conversion

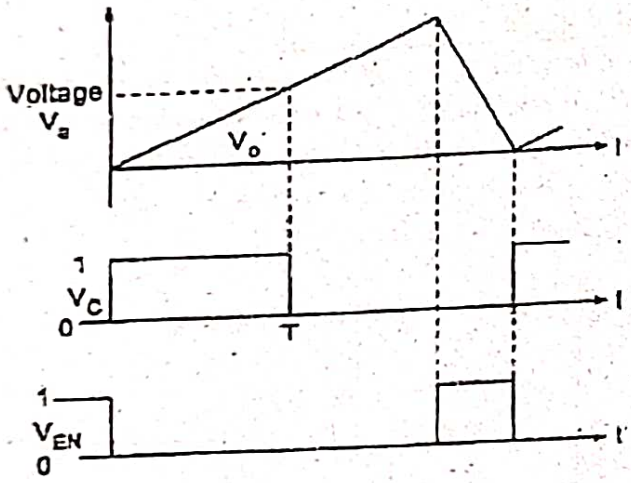


Fig. Conversion process

Q13. Define Oversampling A/D Converter.

Ans. Oversampling ADCs (OSADC) are commonly used in many telecommunications applications such as ADSL. Due to the use of DMT signals in ADSL applications, the requirement on the analog front end (AFE) is generally increased compared with single tone applications. It has also been shown that the linearity is more important than quantization noise for ADCs in DMT applications and OSADCs usually have higher linearity than Nyquist ADCs.

An additional advantage of using OSADCs is the very low quantization noise power at low frequencies, which is beneficial for DMT applications. This is because more bits can be modulated on the lower frequency carriers where the signal is less attenuated by the telephone line. The major drawback of OSADCs is that a relatively high clock frequency must be used if the signal bandwidth is large, making the implementation difficult. Therefore techniques to reduce the oversampling ratio (OSR) of the converter are of interest.

BASICS OF OVERSAMPLING SIGMA-DELTA CONVERTERS : The basic principle behind oversampling sigma-delta modulators is to trade signal bandwidth for resolution. The quantization noise of a low resolution ADC is high-pass filtered to yield a low quantization noise at low frequencies. The noise at high frequencies is removed by a digital filter before the signal is decimated to generate the final output of the converter. A first order sigma-delta modulator is shown in Fig.. It contains an ADC, an integrator, a DAC and a subtractor. The resolution of the ADC is low, usually only 1 bit. The digital output y(nT) is fed back through the DAC and subtracted from the input signal. The output of the subtractor is accumulated in the

integrator and quantized by the ADC. The integrator can be either continuous-time or discrete-time, but a discretetime integrator is more common and will only be considered here. The performance of the modulator can be investigated by using a linear model for the modulator.

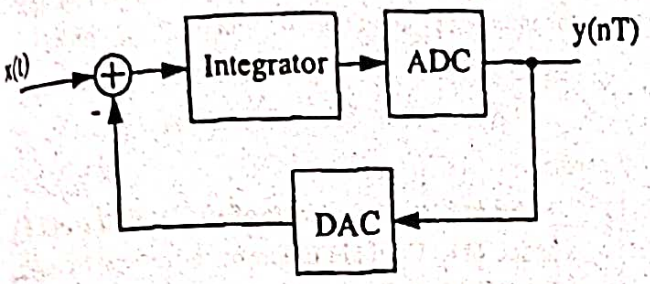


figure : First order sigma-delta modulator.

We assume that the quantization error e(nT) in the ADC is white noise uncorrelated to the input signal.

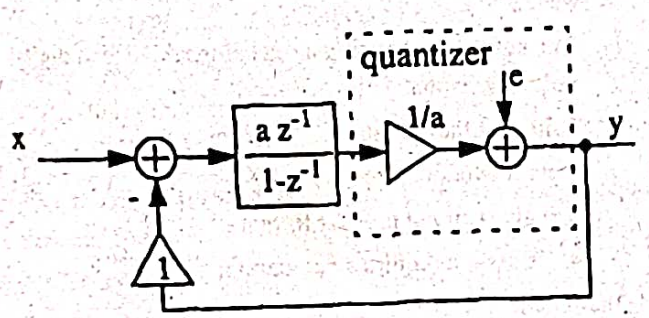


Fig. : Linear model for first order sigma-delta modulator.

A linear model of the modulator is shown in Fig.. If a 1 bit quantizer is used, the gain in the integrator, a , will only affect the voltage swing at the output of the integrator not the output signal. Therefore this gain factor must be compensated for in the linear model of the quantizer. The z-domain output signal is given by

$$Y(z) = z^{-1}.X(z) + (1 - z^{-1}).E(z)$$

Hence the input signal is only delayed while the quantization noise is high-pass filtered. If the signal bandwidth is small compared to the sampling frequency only a small portion of the quantization noise appears in the signal band and a high resolution results. The ratio between the signal bandwidth and the Nyquist frequency is called the oversampling ratio (OSR), i.e.

$$OSR = \frac{f_s/2}{BW}$$

where is the sampling frequency and BW the signal bandwidth.

For the first order modulator the resolution increases by 1.5 bits for every doubling of the sampling frequency. To get a high resolution a very high OSR is needed. The required OSR can be reduced by using a second order modulator. The linear model of a second order modulator is shown in Fig. There are now two integrators in the loop and the output signal is given by

$$Y(z) = z^{-2}.X(z) + (1 - Z^{-1})^2.E(z)$$

OBJECTIVE QUESTIONS AND ANSWERS

1. A 5 bit ladder has a digital input of 11010. Assuming that 0 corresponds to 0 V and 1 corresponds to +10 V, its output voltage will be:

   1.+65V 2.−6.5V
   3.−8.125V 4.+8.125V

Answer : 4

2. The resolution of an 8 bit DAC will be:

   1. 1/255 2. 1/8
   3. 1/128 4. 1/64

Answer : 1

3. A 6-bit ladder D/A converter has a maximum output of 10 V. The output for input 101001 is approximately

   1. 4.2 2. 6.5
   3. 5.5. 4. 9.2

Answer : 2

4. If the resolution of a digital-to-analog converter is approximately 0.4% of its full-scale range, then it is a/an

   1. 1 6-bit converter 2. 10-bit converter
   3. 8-bit converter 4. 12-bit converter

Answer : 3

5. A 8-bit AID converter is used over a span of zero to 2.56 V. The binary representation of 1.0 V signal is

   1. 011 001 00 2. 01110001
   3. 101 001 01 4. 10100010

Answer : 1

6. The resolution of 4 Bit counting ADC is 05 V For an analog input 5.8 volt the output of ADC will be _____
   1. 1100 2. 1111
   3. 1010 4. 1011

Answer : 1

7. A D/A converter has 5V full-scale input voltage and an accuracy of ± 0.2%. The maximum error for any output voltage will be
   1. 5 mV 2. 10 mV
   3. 20 mV 4. 1 mV

Answer : 2

8. A 4-bit R-211 digital to analog converter using Inverting op-amp has a reference of 5V. What is the analog output for the input code 1010?
   1. 3.125V 2. 0.78125 V
   3. –3.125 V 4. 0.3125 V

Answer : 3

9. The present resolution of an 8-bit D/A converter is
   1. 0.392% 2. 1/256
   3. 1/255 4. (A) and (C) both

Answer : 4

10. The difference between analog voltage represented by two adjacent digital codes of an analog to digital converter is
    1. Accuracy 2. Resolution
    3. Quantization 4. Precision

Answer : 2

11. A 10-bit 0/A converter is calibrated over the full range from 0 to 10 V. If the input to the D/A converter is 13A (in hex), the output (rounded off to three decimal places) is _____V

Answer : 3.0 50 – 3.080

12. Minimum number of bits required to represent maximum value of given analogue signal with 0.1% accuracy is:
    1. 8 bits 2. 9 bits
    3. 10 bits 4. 12 bits

Answer : 3

13. Which one of the following analog to digital conversion methods called potentiometric type analog to digital converter?
    1. Successive approximation method
    2. Voltage to time conversion method
    3. Voltage to frequency conversion method
    4. Dual slope integration method

Answer : 1

14. A 5-bit D/A converter has a current output. If an output current $I_{out} = 10$ mA is produced for a digital input of 10100, the value of I_{out} for a digital input of 11101 will be
    1. 12.5 mA 2. 13.5 mA
    3. 15.5 mA 4. 14.5 mA

Answer : 4

15. A 10-bit ADC has a full-scale of 10.230 V when the digital output is $(11\ 1111\ 1111)_2$. The quantization error of the ADC in millivolt is _____.

Answer : 5

16. For a 10-bit digital ramp ADC using 500 kHz clock, the maximum conversion time is
    1 . µs2 I 2. 2064 µs
    3. 2046 µs 4. 2084 µs

Answer : 3

17. The advantage of using a dual slope ADC in a digital voltmeter is that
    1. its accuracy is high
    2. its conversion time is small
    3. it gives output in BCD format
    4. it does not require a comparator

Answer : 1

18. Maximum value of signal to noise ratio of an 8 bit ADC with an UP range of 10 V will be
    1. 50 dB 2. 43.8 dB
    3. 48.9 dB 4. 49.8 dB

Answer : 4

19. Assume worst case SNR of a 10 bit ADC is 57 dB. If the resolution is increased by 2 bits, the resulting SNR will be approximately
    1. 67 dB 2. 69 dB
    3. 45 dB 4. 74 dB

Answer : 2

20. A Dual slope ADC has C = 0.34 nanofarad and R = 1 KΩ has charging and discharging time for some voltage of 12 ns and 9 ns respectively. The reference Voltage is 2.5

V. What will be the peak voltage reached by triangular wave during charging?

1. 0.066V
2. 7.0004 V
3. 6.0984 V
4. 0.2347 V

Answer : 1

21. Among the following four, the slowest ADC (analog-to-digital converter) is

1. parallel-comparator (flash) type
2. Successive approximation type
3. Integrating type
4. Counting type

Answer : 3

22. In dual slope type of ADCs, an input hold time is

1. Almost zero
2. Higher than that of flash type ADCs
3. Longest
4. All of the above

Answer : 2

23. The fastest type of Analog to Digital converter is

1. Counter type
2. Tracking type
3. Successive approximation type
4. Parallel comparator type

Answer : 4

24. Find the resolution of a 10-bit AD converter for an input range of 10 V.

1. 97.7 mV
2. 9.77 mV
3. 0.977 mV
4. 977 mV

Answer : 2

25. An 8-bit, unipolar successive approximation Register type ADC is used to convert 3.5 V to digital equivalent output. The reference voltage is +5V. The output of the ADC at the end of third clock pulse after start of conversion, is

1. 10100000
2. 10000000
3. 00000001
4. 00000011

Answer : 1

26. Which of the following is NOT one of the analog to digital (AID) conversion techniques?

1. Single slope integration method
2. Successive approximation method
3. Voltage to-lime conversion method
4. Voltage to frequency conversion method

Answer : 1

27. In which of the following types of AID converter does the conversion time almost double for every bit added to the device?

1. Counter type A/D converter
2. Tracking type A/D converter
3. Single-slope integrating type A/D converter
4. Successive approximation type A/D converter

Answer : 1

28. A 6-bit ADC has a maximum precision supply voltage of 20 V. What are the voltage changes for each LSB present and voltage to be presented by (100110), respectively?

1. 0.317V and 12.06 V
2. 3.17V and 12.06V
3. 0.317V and 1.206V
4. 3.17V and 1.206V

Answer : 1

29. A temperature in the range of –40° C to 55° C is to be measured with a resolution of 0.10 C. The minimum number of ADC bits required to get a matching dynamic range of the temperature sensor is

1. 8
2. 10
3. 12
4. 14

Answer : 2

30. The number of comparators in a 4 bit flash ADC is

1. 4
2. 5
3. 15
4. 16

Answer : 3

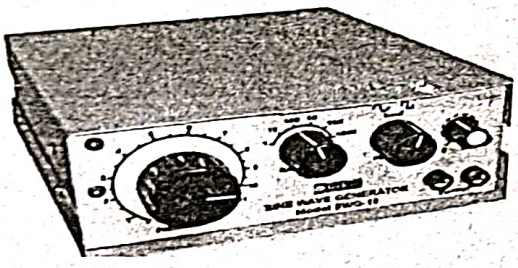
UNIT 05

WAVEFORM GENERATORS AND SPECIAL FUNCTION ICs

QUESTIONS AND ANSWERS

Q1. Explain Sine Wave Generator ? and write its working principle.

Ans. A circuit that is used to generate a sine wave is called a sine wave generator. This is one kind of waveform that appears from electricity outlets of home. This waveform can be observed in AC power as well as applicable in acoustics. We know that there are different types of waveforms that are generated by different electronic devices. So each waveform generates different sounds. A sine wave is one kind of signal that is utilized in acoustics. To design the sine wave generator circuit, there are different types of components are required like an integrated circuit, resistors, capacitors, transistors, etc.

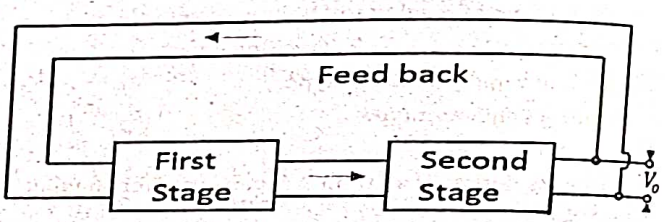


Sine Wave Generator

Working Principle : *This is an outstanding tool to generate sine waves using wave drivers otherwise speakers. The frequency range of this generator will range from 1Hz to 800 Hz & the sine wave's amplitude to be changed. Students can notice the nature of quantum for standing wave models when the sine wave generator jumps from one resonant frequency to others. This generator includes in-built memory that permits it to find out the latest and primary frequencies for extra exploration.*

Q2. What is a Multivibrator?

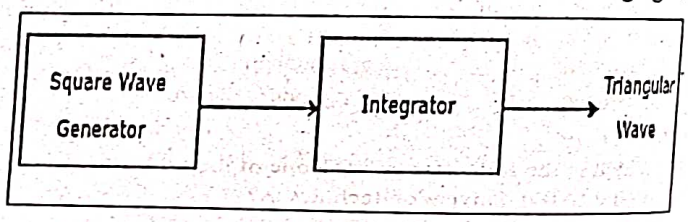
Ans. According to the definition, A Multivibrator is a two-stage resistance coupled amplifier with positive feedback from the output of one amplifier to the input of the other. Two transistors are connected in feedback so that one controls the state of the other. Hence the ON and OFF states of the whole circuit, and the time periods for which the transistors are driven into saturation or cut off are controlled by the conditions of the circuit. The following figure shows the block diagram of a Multivibrator.



Block Diagram

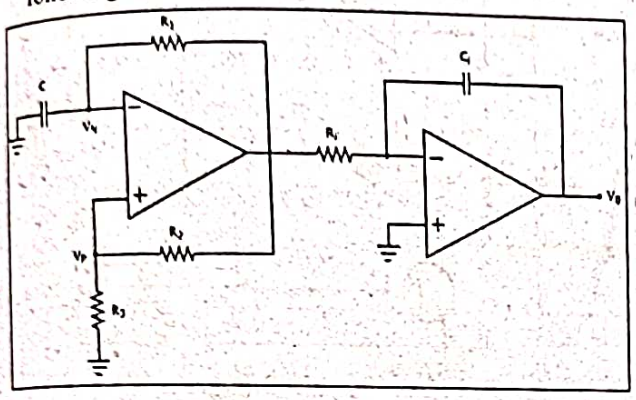
Q3. Define Triangular Wave Generator with the help of suitable diagrams.

Ans. A triangular wave generator is an electronic circuit, which generates a triangular wave. The block diagram of a triangular wave generator is shown in the following figure



The block diagram of a triangular wave generator contains mainly two blocks: a square wave generator and an integrator. These two blocks are cascaded. That means, the output of square wave generator is applied as an input

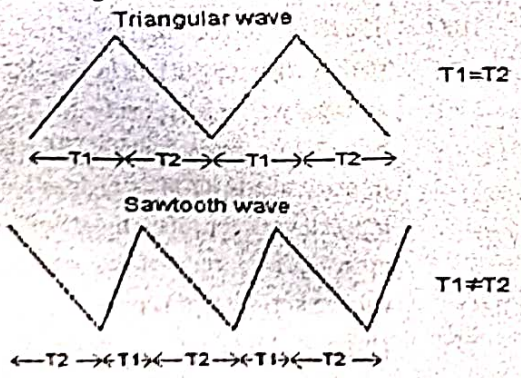
of integrator. Note that the integration of a square wave is nothing but a triangular wave.The circuit diagram of an op-amp based triangular wave generator is shown in the following figure -



We have already seen the circuit diagrams of a square wave generator and an integrator. Observe that we got the above circuit diagram of an op-amp based triangular wave generator by replacing the blocks with the respective circuit diagrams in the block diagram of a triangular wave generator.

Q4. Explain Sawtooth Wave Generator.

Ans. A linear, non-sinusoidal, triangular shape waveform represents a sawtooth waveform in which fall time and rise time are different. A linear, non-sinusoidal, triangular shape waveform represents a pure triangular waveform in which fall time and rise times are equal. The Sawtooth Wave Generator is also known as an asymmetric triangular waveform. The graphical representation of a sawtooth waveform is given below:



Sawtooth Wave Generator

The applications of a sawtooth waveform are in frequency/ tone generation, sampling, thyristor switching, modulation, etc. A non-sinusoidal waveform is nothing but a sawtooth waveform. Because its teeth look like a saw, it is named as a sawtooth waveform. In an inverse (or reverse) sawtooth waveform the wave suddenly ramps downwards and then rises sharply.

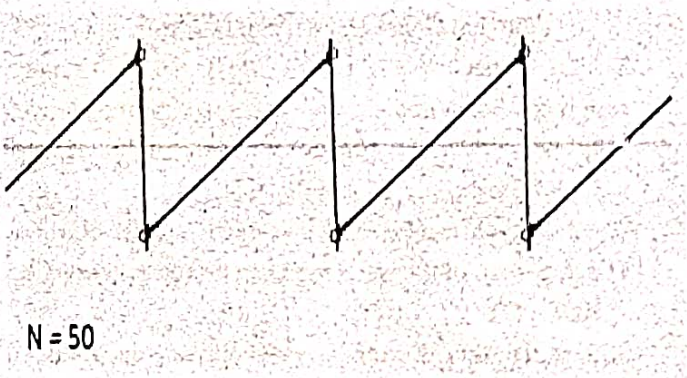
The infinite Fourier series is .

$$x_{reversesawtooth}(t) = 2A/\pi \sum_{K=1}^{\infty} (-1)^k \sin(2\pi kft)$$

A conventional sawtooth can be constructed using

$$x_{sawtooth}(t) = \frac{A}{2} - \frac{A}{\pi} \sum_{K=1}^{\infty} \frac{\sin(2\pi kft)}{k}$$

Where A is the amplitude : By using a fast Fourier transform, this summation can be calculated more efficiently. In the time domain, the waveform is digitally created by using the non-band limited form. Sampling the infinite harmonics results in the tone that contains aliasing distortion.

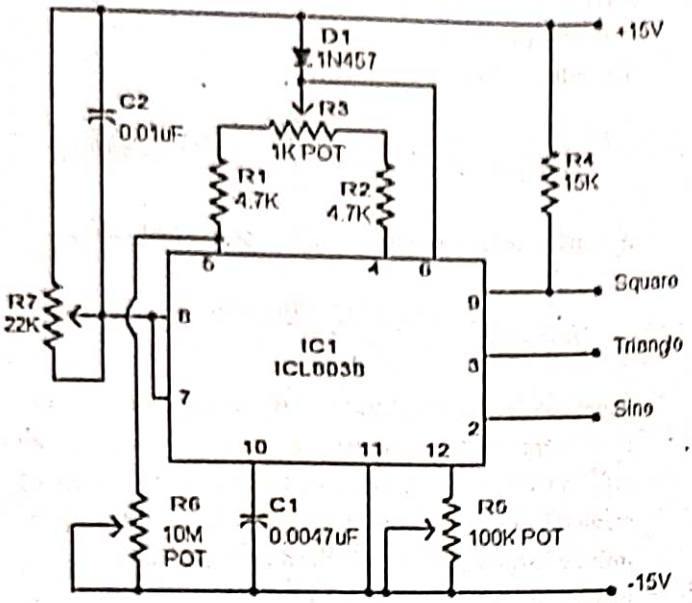


Synthesis Sawtooth

Q5. Describe ICL8038 function generator.

Ans. The ICL8038 is a function generator chip, capable of generating triangular, square , sine, pulse and sawtooth waveforms . From these sine, square & triangular wave forms can be made simultaneously.There is an option to control the parameters like frequency,duty cycle and distortion of these functions.This is the best function generator circuit for a beginner to start with and is of course a must on the work bench of an electronics hobbyist.The circuit here is designed to produce waveforms from 20Hz to 20 kHz.The

ICL 8038 has to be operated from a dual power supply

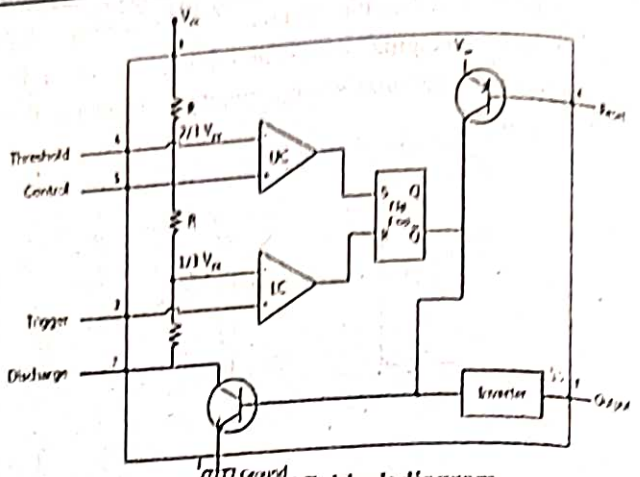


Function Generator Circuit Diagram

- The circuit needs a dual power supply. A +15 –15 power supply as shown in the circuit is enough for the purpose.
- The frequency of the output wave form can be adjusted using R7.It must be a 100K Log POT.
- The duty cycle can be adjusted using R3 , a 1K POT.
- The distortion of the wave form can be adjusted using R5 , a 100K POT.
- Square,triangle & sine waveforms can be obtained simultaneously at pins 9,3,2 respectively.

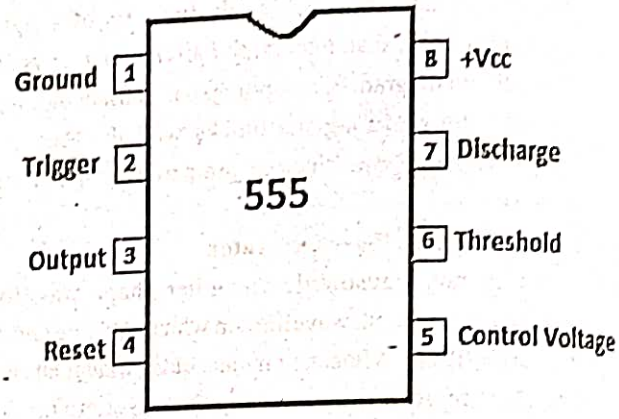
Q6. Explain the IC 555 Timer also sketch the its Pin Diagram and write Specifications.

Ans. The 555 timer IC is an integral part of electronics projects. Be it a simple project involving a single 8-bit micro-controller and some peripherals or a complex one involving system on chips (SoCs), 555 timer working is involved. These provide time delays, as an oscillator and as a flip-flop element among other applications.Depending on the manufacturer, the standard 555 timer package includes 25 transistors, 2 diodes and 15 resistors on a silicon chip installed in an 8-pin mini dual-in-line package (DIP-8). Variants consist of combining multiple chips on one board. However, 555 is still the most popular. Let us look at the pin diagram to have an idea about the timer Integrated Circuit (IC) before we talk about 555 timer working.



555 Timer IC: block diagram

555 timer working: pin configuration.



8 pin DIP configuration

P In diagram and description :

Pin	Name	Purpose
1	GND	Ground reference voltage, low level (0 V)
2	TRIG	The OUT pin goes high and a timing interval starts when this input falls below 1/2 of CTRL voltage (which is typically 1/3 Vcc, CTRL being 2/3 Vcc by de fault if CTRL is left open). In other words, OUT is high as long as the trigger low. Output of the timer totally depends upon the amplitude of the external trigger voltage applied to this pin.
3	OUT	This output is driven to approximately 1.7 V below +Vcc, or to GND.
4	RESET	A timing interval may be reset by driving this input to GND, but the timing does not begin again until RESET rises above approximately 0.7 volts. Over rides TRIG which overrides threshold.

5	CTRL	Provides "control" access to the internal voltage divider (by default, 2/3 Vcc).
6	THR	The timing (OUT high) interval ends when the voltage at threshold is greater than that at CTRL (2/3 Vcc if CTRL is open).
7	DIS	Open collector output which may discharge a capacitor between intervals. In phase with output.
3	Vcc	Positive supply voltage, which is usually between 3 and 15 V depending on the variation.

Some important features / Specifications of the 555 timer:

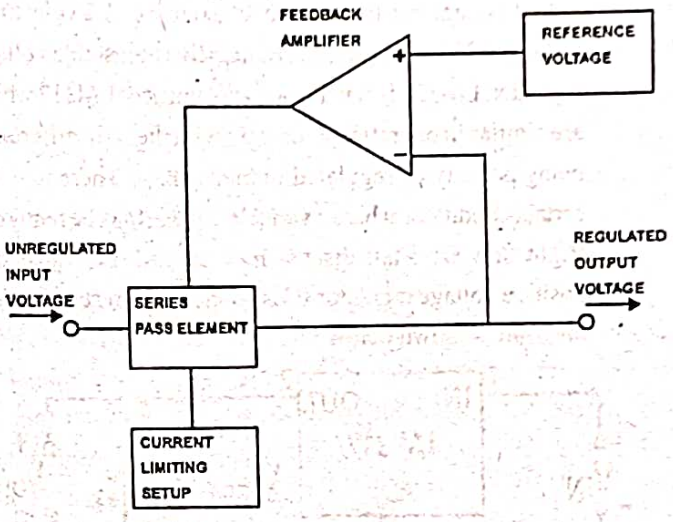
555 timer is used in almost every electronic circuit today. For a 555 timer working as a flip flop or as a multi-vibrator, it has a particular set of configurations. Some of the major features of the 555 timer would be,

- It operates from a wide range of power ranging from +5 Volts to +18 Volts supply voltage.
  Sinking or sourcing 200 mA of load current.
- The external components should be selected properly so that the timing intervals can be made into several minutes along with the frequencies exceeding several hundred kilohertz.
- The output pin of a 555 timer can drive a transistor-transistor logic (TTL) due to its high current output.
- It has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature which is equivalent to 0.005 %/ °C.
- The duty cycle of the timer is adjustable.
  Also, the maximum power dissipation per package is 600 mW and its trigger pulse and reset inputs has logic compatibility.

Q7. Describe IC Voltage Regulators.

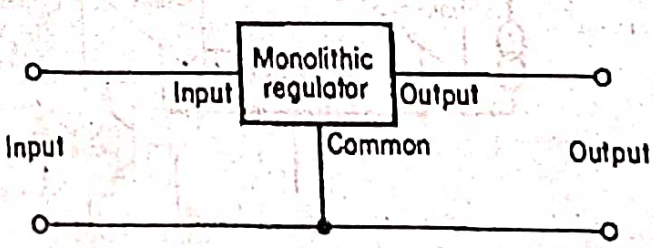
Ans. A voltage regulator is one of the most widely used electronic circuitry in any device. A regulated voltage (without fluctuations & noise levels) is very important for the smooth functioning of many digital electronic devices. A common case is with micro controllers, where a smooth regulated input voltage must be supplied for the micro controller to function smoothly. Voltage regulators are of different types. In this article, our interest is only with IC based voltage regulator. An example of IC based voltage regulator available in market is the popular 7805 IC which regulates the output voltage at 5 volts. Now lets come to the basic definition of an IC voltage regulator. It is an integrated circuit whose basic purpose is to regulate the unregulated input voltage (definitely over a predefined range) and provide with a constant, regulated output voltage.

BLOCK DIAGRAM OF IC VOLTAGE REGULATOR



Q8. Explain Three terminal fixed and adjustable voltage regulators.

Ans. *Fixed Voltage Regulators* : These regulators provide a constant output voltage. A popular example is the 7805 IC which provides a constant 5 volts output. A fixed voltage regulator can be a positive voltage regulator or a negative voltage regulator. A positive voltage regulator provides with constant positive output voltage. All those IC's in the 78XX series are fixed positive voltage regulators. In the IC nomenclature – 78XX ; the part XX denotes the regulated output voltage the IC is designed for. Examples:- 7805, 7806, 7809 etc. A negative fixed voltage regulator is same as the positive fixed voltage regulator in design, construction & operation. The only difference is in the polarity of output voltages. These IC's are designed to provide a negative output voltage. Example:- 7905, 7906 and all those IC's in the 79XX series.



Adjustable Voltage Regulator : An adjustable voltage regulator is a kind of regulator whose regulated output voltage can be varied over a range. There are two variations of the same; known as positive adjustable voltage regulator and negative adjustable regulator. LM317 is a classic example of positive adjustable voltage regulator, whose output voltage can be varied over a range of 1.2 volts to 57 volts. LM337 is an example of negative adjustable voltage regulator. LM337 is actually a complement of LM317 which are similar in operation & design; with the only difference being polarity of regulated output voltage.There may be certain conditions where a variable voltage may be required. Right now we shall discuss how an LM317 adjustable positive voltage regulator IC is connected. The connection diagram is shown below.

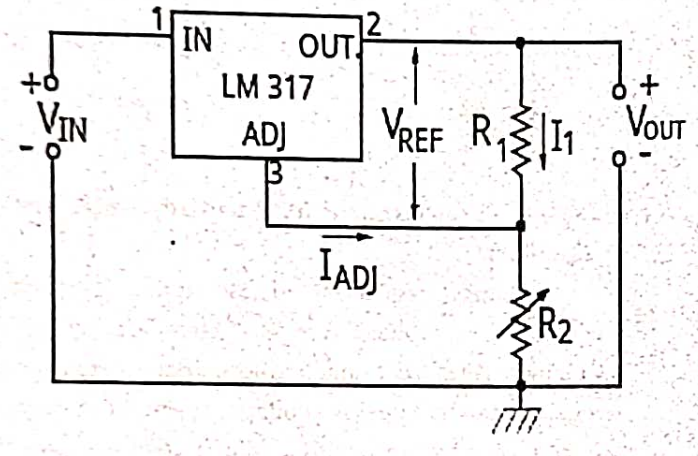
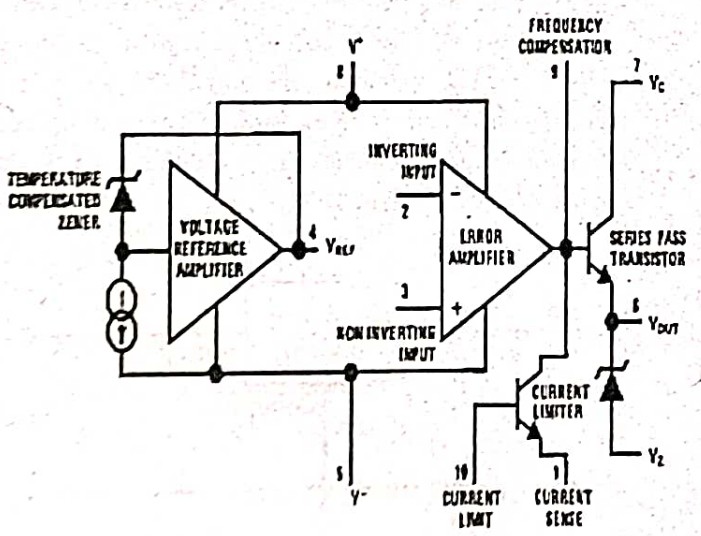


Fig. Adjustable Voltage Regulator using LM317

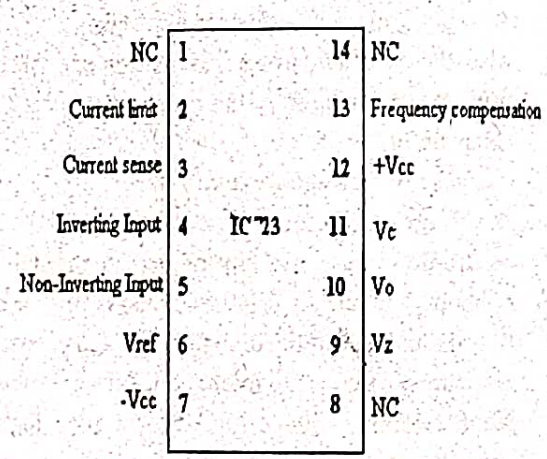
Q9. Define IC 723 General Purpose Regulator and write its features.

Ans. The simplified functional block diagram can be divided in to 4 blocks.



1. **Reference Generating block :** The temperature compensated Zener diode, constant current source & voltage reference amplifier together from the reference generating block. The Zener diode is used to generate a fixed reference voltage internally. Constant current source will make the Zener diode to operate at affixed point & it is applied to the Non – inverting terminal of error amplifier. The Unregulated input voltage ±Vcc is applied to the voltage reference amplifier as well as error amplifier.
2. **Error Amplifier :** Error amplifier is a high gain differential amplifier with 2 input (inverting & Non-inverting). The Non-inverting terminal is connected to the internally generated reference voltage. The Inverting terminal is connected to the full regulated output voltage.
3. **Series Pass Transistor :** Q1 is the internal series pass transistor which is driven by the error amplifier. This transistor actually acts as a variable resistor & regulates the output voltage. The collector of transistor Q1 is connected to the Un-regulated power supply. The maximum collector voltage of Q1 is limited to 36Volts. The maximum current which can be supplied by Q1 is 150mA.
4. **Circuitry to limit the current :** The internal transistor Q2 is used for current sensing & limiting. Q2 is normally OFF transistor. It turns ON when the IL exceeds a predetermined limit.

Low voltage, Low current is capable of supplying load voltage which is equal to or between 2 to 7Volts.
Vload = 2 to 7V and Iload = 50mA



Features of IC723:

1. Unregulated dc supply voltage at the input between 9.5V &40V
2. Adjustable regulated output voltage between 2 to 3V.
3. Maximum load current of 150 mA (ILmax = 150mA).

4. With the additional transistor used, ILmax upto 10A is obtainable.
5. Positive or Negative supply operation
6. Internal Power dissipation of 800mW.
7. Built in short circuit protection.
8. Very low temperature drift.
9. High ripple rejection.

Q10. Monolithic Switching Regulator.

Ans. The µA78S40 consists of a temperature compensated voltage reference, duty cycle controllable oscillator with an active current limit circuit, a high gain comparator, a high- current, high voltage output switch, a power switching diode & an uncommitted op-amp. Important features of the µA78S40 switching regulators are:

- Step up, down & Inverting operation
- Operation from 2.5 to 40V input
- 80dB line & load regulations
- Output adjustable from 1.3 to 40V
- Peak current to 1.5A without external resistors
- Variable frequency, variable duty cycle device

The internal switching frequency is set by the timing capacitor CT, connected between pin12 & ground pin 11. The initial duty cycle is 6:1. The switching frequency & duty cycle can be modified by the current limit circuitry, IPK sense, pin14, 7 the comparator, pin9 & 10.

Comparator : The comparator modifies the OFF time of the output switch transistor Q1 & Q2. In the step – up & step down modes, the non-inverting input(pin9) of the comparator is connected to the voltage reference of 1.3V (pin8) & the inverting input (pin10) is connected to the output terminal via the voltage divider network.

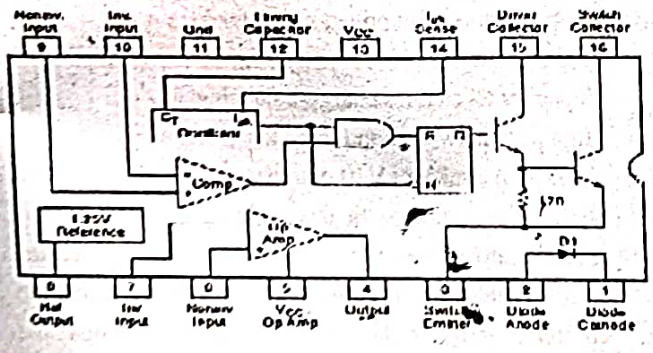


Fig. Functional block diagram of µA78S40

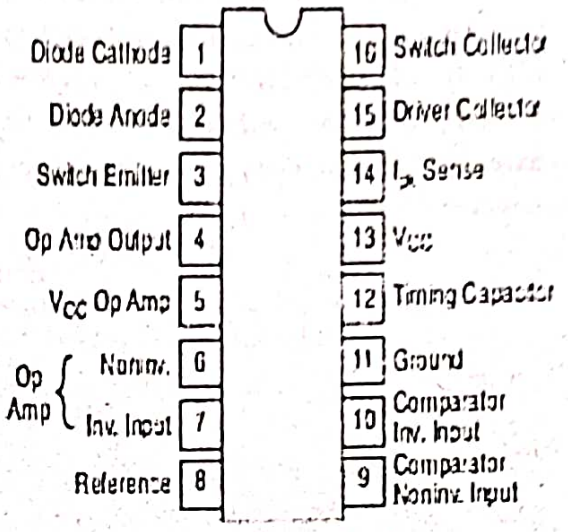


Fig. Pin diagram of Monolithic Switching Regulator.

In the Inverting mode the non – inverting input is connected to both the voltage reference & the output terminal through 2 resistors & the inverting terminal is connected to ground.

When the output voltage is correct, the comparator output is in high state & has no effect on the circuit operation.

However, if the output is too high & the voltage at the inverting terminal is higher than that at the non-inverting terminal, then the comparator output goes low.

In the LOW state the comparator inhibits the turn on of the output switching transistors. This means that, as long as the comparator output is low, the system is in off time.

As the output current rises or the output voltage falls, the off time of the system decreases.

Consequently, as the output current nears its maximum IoMAX, the off time approaches its minimum value.

In all 3 modes (Step down, step up, Inverting), the current limit circuit is completed by connecting a sense resistor Rsc, between IPK sense & Vcc.

The current limit circuit is activated when a 330mV potential appears across Rsc.

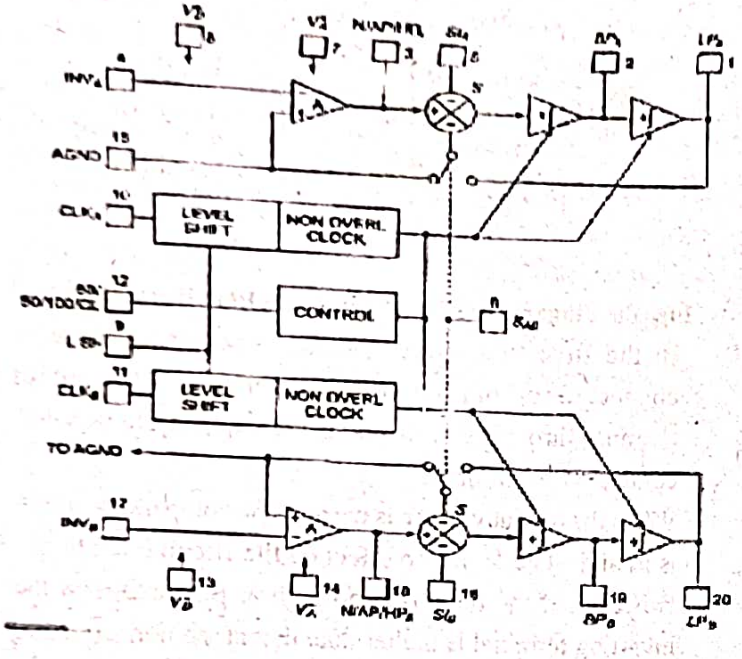
Rsc is selected such that 330mV appears across it when the desired peak current IPK, flows through it.

When the peak current is reached, the current limit circuit is turned on.

The forward voltage drop, VD, across the internal power diode is used to determine the value of inductor L off time & efficiency of the switching regulator.

Q. Explain Switched Capacitor Filter ICs MF10.

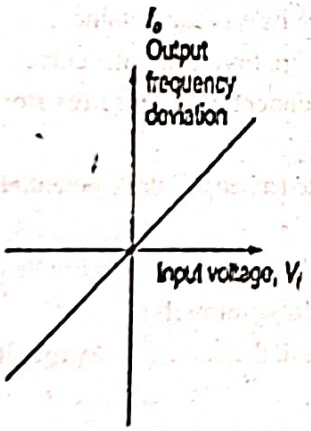
Ans. Switched capacitor filter MF10 : The MF10 contains two of the second-order universal filter sections found in the MF5. Therefore with MF10, two second order filters or one fourth-order filter can be built. As the MF5 and MF10 have similar filter sections, the design procedure for them is same.

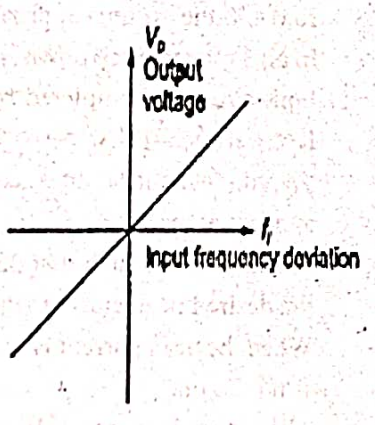


Q11. Explain Frequency to Voltage (F-V) and voltage to frequency (V-F) convertors.

Ans. *Frequency to Voltage convertors (F-V) :*

- F-V convertors applications: Tachometer in motor speed control Rotational speed measurement.
- Two types of it: Pulse integrating Phase locked loop





- F-V convertor produces an output voltage whose amplitude is a function of input signal frequency.
- V0 = kf fi kf is sensitivity of F-V convertor
- It is basically a FM discriminator.

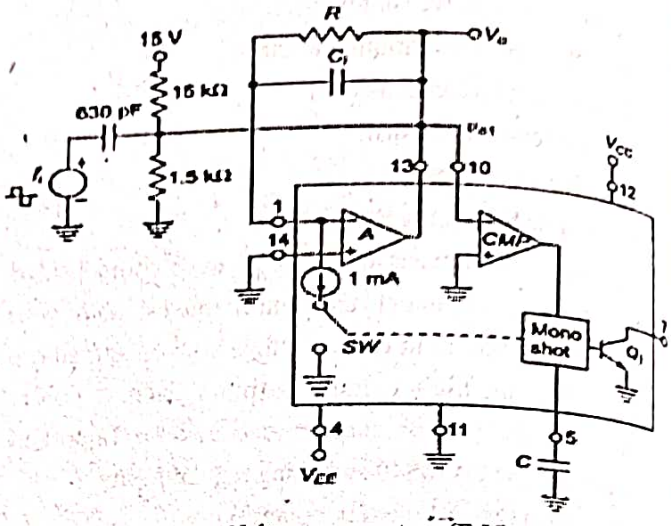


Fig. Frequency to Voltage convertors (F-V) using (VFC32)

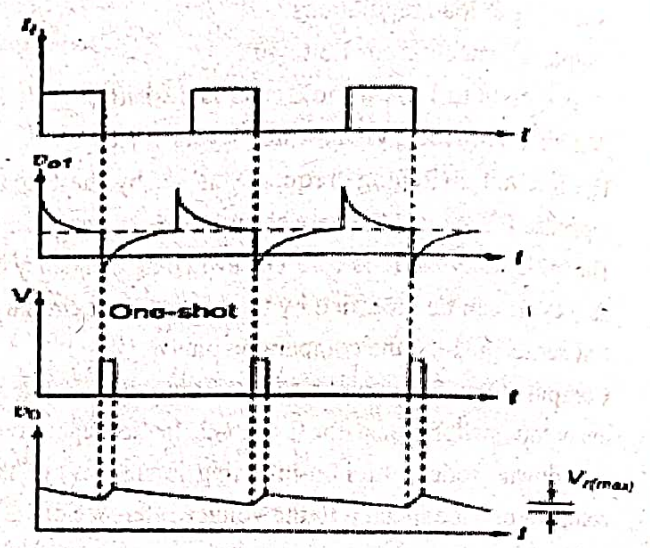


Fig. (F-V) convertors using (VFC32) I/P O/P Graph

Input frequency is applied to comparator A.

Resistor R acts as feedback element.

Capacitor Ci enables charge-balancing,

High pass network conditions input signal

For negative spike of V 01, comparator COMP triggers one shot multivibrator with threshold 7.5V The output of multivibrator closes the switch SW, for a time TH, this causes voltage Vo to build up and inject thru R and this continues until current out of summing input of opamp is equal to that injected by Vo through R continuously.

Vo=10-3 *TH *R*fi as TH =7.5 C /1X10-3

Ripple Voltage, Vr(max) =7.5 C /Ci

Voltage to frequency convertor :

Principle: Charge balancing technique-the process of charging and discharging results in frequency proportional to input signal F0= k Vi

When switch SW is open the current flows into capacitor Ci and charges it, and node voltage Vo1 produce ramp down.

When V01 =0 CMP triggers and sends a triggering signal to one shot multivibrator that closes the switch SW and turns transistor Q ON for time TH.

The threshold of mono shot = 7.5 V and

$$TH = 7.5\,C/10-3$$

During TH , V01 ramps upward by amount

$$\delta V01 = (1mA - Ii)\,TH/Ci$$

Time duration TL for vo1 to return to 0 is

$$TL = C\,\delta V01/Ii$$

$$TL + TH = 1mA\,TH/Ii = T$$

$$F0 = Vi/7.5\,RC$$

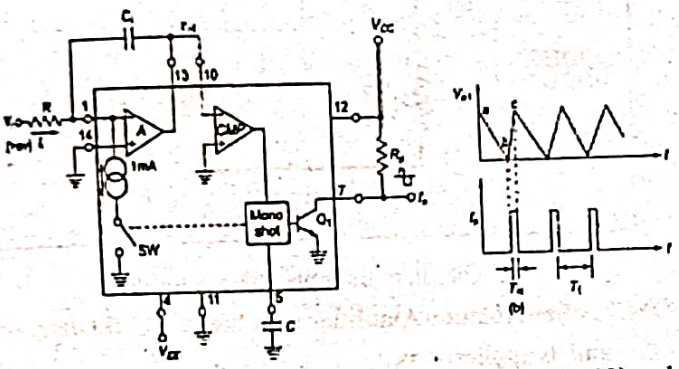


Fig. Voltage to Frequency convertors (F-V) using (VF32) and I/P O/P Graph

Q12. Describe Power Audio Amplifier IC LM 380.

Ans. Small signal amplifiers are essentially voltage amplifier that supplies their loads with larger amplifier signal voltage.On the other hand, large signal or power amplifier supply a large signal current to current operated loads such as speakers & motors.

In audio applications, however, the amplifier called upon to deliver much higher current than that supplied by general purpose op-amps. This means that loads such as speakers & motors requiring substantial currents cannot be driven directly by the output of general purpose op-amps. To handle it following is done

- To use discrete or monolithic power transistors called power boosters at the output of the op-amp
- To use specialized ICs designed as power amplifiers like LM380.

Features of LM380:

1. Internally fixed gain of 50 (34dB)
2. Output is automatically self centering to one half of the supply voltage.
3. Output is short circuit proof with internal thermal limiting.
4. Input stage allows the input to be ground referenced or ac
5. Wide supply voltage range (5 to 22V).
6. High peak current capability.
7. High impedance.

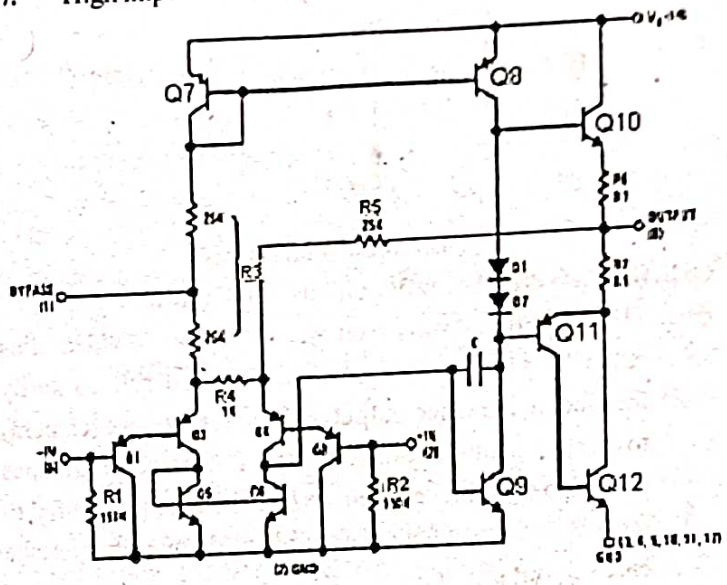


Fig. Funtional block diagram of Power Audio Amplifier

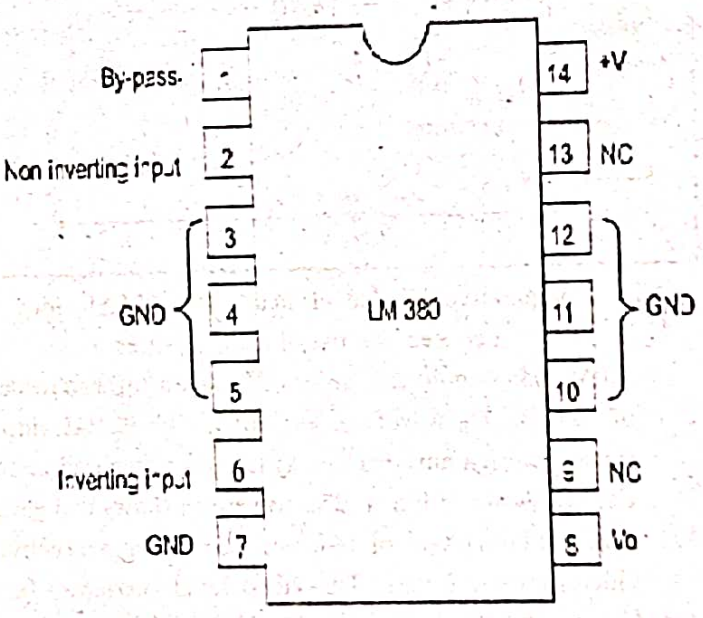


Fig. Pin diagram of Power Audio Amplifier LM 380

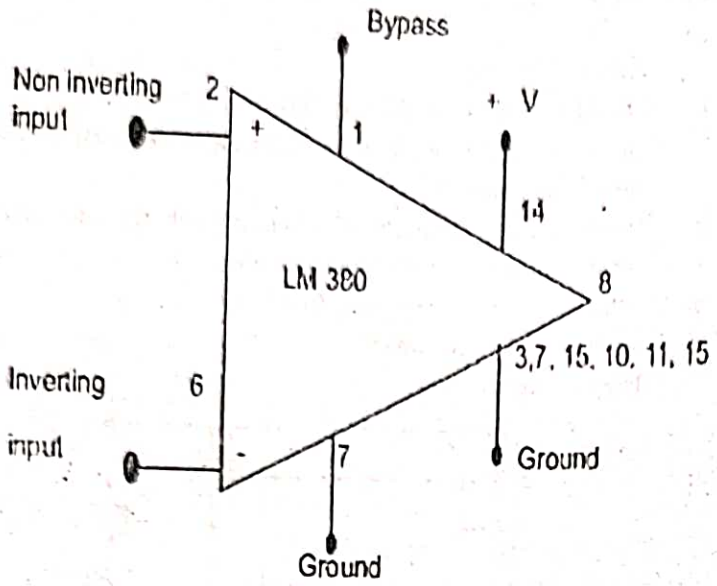


Fig. Block diagram LM380

Q13. Define Video Amplifier and its ckt diagram.

Ans. There are times when you want to view the video clips taken by your camera on your TV. You can do so by interfacing the video output of the source device (camera) to the video input terminals of the TV. However, at times the video signal level needs to be raised before it is fed to the TV. Presented here is a simple video amplifier to take care of your problems.

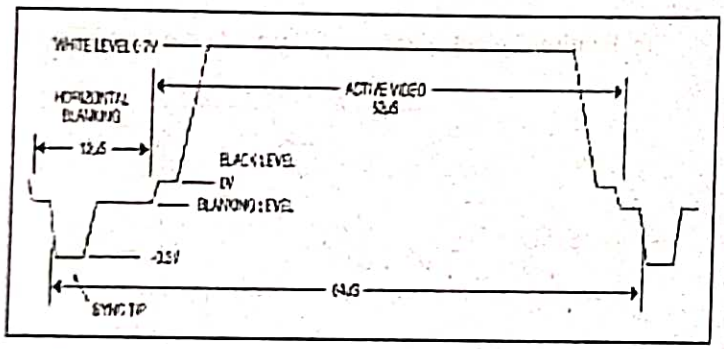


Fig. : Comparative signal levels in a 1VPK-PK PAL video between any two line sync pulses

A PAL video amplifier is expected to have a 3dB bandwidth of 5.5 MHz. The waveform levels of a 1VPk-Pk PAL video signal between any two line sync pulses (separation 64 Us) are shown in Fig. 1. The waveform shows that each scan line lasts 64 µs, of which only 52 Uscontains active video or picture data. The video level (variable) lies between 0V and 0.7V and the blanking level extends from 0V down to –0.3V (for 12 Us). The black level or blanking level starts at 0V, the white level or peak video level is 0.7V and the sync pulse peak (-ve) level is –0.3V.

A simple video amplifier circuit :The R1-R2 divider network adjusts the DC level of the video, while the R5-R6 divider network adjusts the gain. You may replace both the dividers with two 4.7-kilo-ohm (or 5-kilo-ohm) trimpots for proper adjustment of the DC level and the gain. The 75-ohm resistor (R3) may be discarded if you feed the video from a high-output-impedance stage.

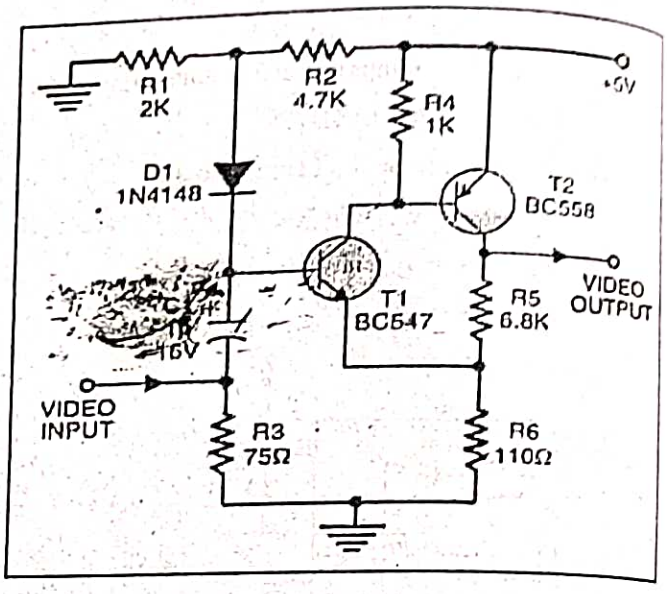


Fig. : Circuit of a simple video amplifier

Q14. Define Isolation Amplifier with the help of ckt diagram and its applications.

Ans. An isolation amplifier or a unity gain amplifier provides isolation from one fraction of the circuit to another fraction. So, the power cannot be drawn, used and wasted within the circuit. The main function of this amplifier is to increase the signal. The same input signal of the op-amp is passed out exactly from the op-amp as an output signal. These amplifiers are used to give an electrical safety battier as well as isolation. These amplifiers protect the patients from the outflow of current. They crack electrical signal's ohmic continuity among input & output and isolated power supply can be provided for both the input and output. So, the low-level signals can be amplified. An isolation amplifier can be defined as, an amplifier which doesn't have any conductive contact among input as well as output sections. Consequently, this amplifier gives ohmic isolation among the i/p & o/p terminals of the amplifier. This isolation must

have less leakage as well as a high amount of dielectric breakdown voltage. The typical resistor and capacitor values of amplifier among the input & output terminals are resistor should have 10 Tera Ohms and capacitor should have 10 picofarads.

Fig. Isolation-amplifier

These amplifiers are frequently used when there is extremely huge common-mode voltage disparity among input & output side. In this amplifier, the ohmic circuitry is not there from input ground to output ground.

When the input impedance of an op-amp is extremely high then the isolation can be caused. As this circuit includes high input impedance, then minute current can be drawn from the amplifier circuit. According to Ohms law, when the resistance is high, then the current will be drawn less from the power supply.

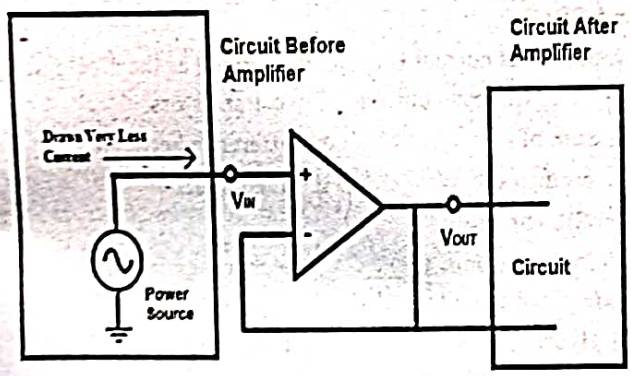


Fig. Isolation-amplifier circuit diagram

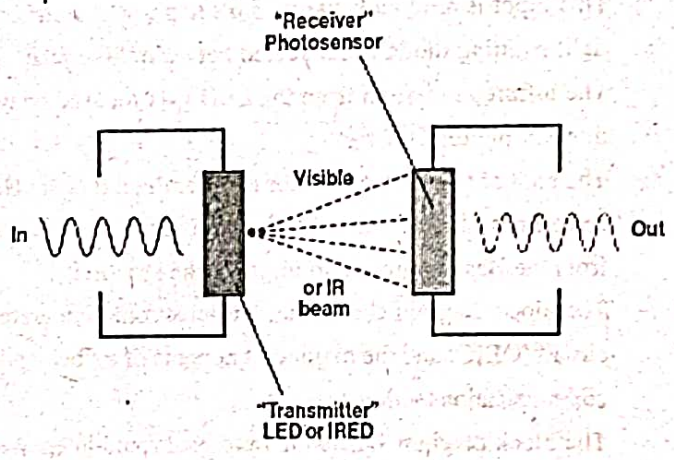
Therefore, an op-amp does not draw a significant quantity of current from the power source. So in practice, there is no current will be drawn as well as transferred from one portion to another portion of the circuit. Therefore, this amplifier works as an isolation device.When the input impedance of an op-amp is low then it draws a vast amount of current.

Isolation Amplifier Applications :

1. These amplifiers are normally used in applications like signal conditioning. This may utilize different bipolar, CMOS, & complementary bipolar amplifiers which include chopper, isolation, instrumentation amplifiers.
2. As several devices work by using low power sources otherwise batteries. Selecting an isolation amplifier for different applications mainly depends on the supply voltage characteristics of an amplifier.

Q15. What is an Optocoupler ? Brief its working.

Ans. An optocoupler (also called optoisolator) is a semiconductor device that allows an electrical signal to be transmitted between two isolated circuits. Two parts are used in an optocoupler: an LED that emits infrared light and a photosensitive device that detects light from the LED. Both parts are contained within a black box with pins for connectivity. The input circuit takes the incoming signal, whether the signal is AC or DC, and uses the signal to turn on the LED.The photosensor is the output circuit that detects the light and depending on the type of output circuit, the output will be AC or DC. Current is first applied to the optocoupler, making the LED emit an infrared light proportional to the current going through the device. When the light hits the photosensor a current is conducted, and it is switched on. When the current flowing through the LED is interrupted, the IR beam is cut-off, causing the photosensor to stop conducting.



Working of Optocoupler Configuration : The term optocoupler and optoisolator are often used interchangeably, but there is a slight difference between

the two. The distinguishing factor is the voltage difference expected between the input and the output. The optocoupler is used to transmit analog or digital information between circuits while maintaining electrical isolation at potentials up to 5,000 volts. An optoisolator is used to transmit analog or digital information between circuits where the potential difference is above 5,000 volts.

Q16. Explain Opto coupler IC / fibre optic IC.

Ans.

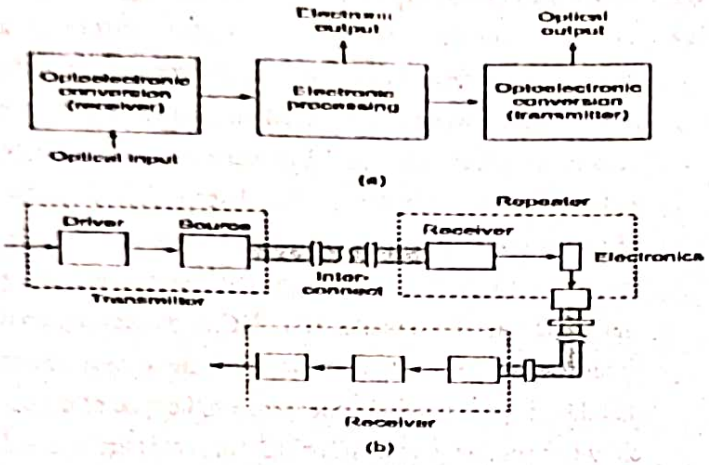


Fig. The block diagram of Opto coupler IC / fibre optic IC.

The optocouplers are available in the IC form MCT2E is the standard optocoupler IC which is used popularly in many electronic application.

- This input is applied between pin 1& pin 2. An infrared light emitting diode is connected between these pins.
- The infrared radiation from the LED gets focused on the internal phototransistor.
- The base of the phototransistor is generally left open. But sometimes a high value pull down resistance is connected from the Base to ground to improve the sensitivity.
- The block diagram shows the opto-electronic-integrated circuit (OEIC) and the major components of a fiber-optic communication facility.
- The block diagram shows the opto-electronic-integrated circuit (OEIC) and the major components of a fiber-optic communication facility.

OBJECTIVE QUESTIONS AND ANSWERS

1) Which among the following is/are the feature/s characteristic/s of an integrated op-amp?
   a. Small size
   b. High reliability
   c. Low cost & less power consumption
   d. All of the above

ANSWER: (d)

2) In a typical op-amp, which stage is supposed to be a dual-input unbalanced output or single-ended output differential amplifier?
   a. Input stage
   b. Intermediate stage
   c. Output stage
   d. Level shifting stage

ANSWER: (b)

3) In differential mode of op-amp, if output voltage is equal to the difference between outputs of individual transistors, its amplitude will be _____the amplitude of signal voltage yielded at collector to ground.
   a. twice
   b. thrice
   c. four times
   d. one-fourth times

ANSWER: (a)

4) In a differential amplifier, the configuration is said to be an 'unbalanced output', if _____
   a. Output voltage is measured between two collectors
   b. Output is measured with respect to ground
   c. Two input signals are used
   d. All of the above

ANSWER: (b)

5) Input offset current is basically defined as the algebraic _____ the base current of two transistors.
   a. sum of
   b. difference between
   c. product of
   d. division of

ANSWER: (b)

6) Unipolar belongs to _____technology/ies of integrated circuits.
   a. Hybrid
   b. Monolithic
   c. Both a and b
   d. None of the above

ANSWER: (b)

7) Which among the following belong to the category of bipolar technology?
   A. JFET
   B. MOSFET
   C. P-N junction isolation
   D. Di-electric isolation

a. A & B b. B & C
c. C & D d. A & D

ANSWER: (c)

8) Which op-amp technology/ics exhibit/s low current sourcing/ sinking capacity?
a. Bipolar op-amp b. CMOS op-amp
c. BICMOS op-amp d. All of the above

ANSWER: (b)

9) How many stages are involved in bipolar op-amp?
a. 2 b. 3
c. 4 d. 6

ANSWER: (b)

10) In op-amps, which type of noise occurs due to discrete flow of current in the device?
a. Shot noise b. Burst noise
c. Thermal noise d. Flicker noise

ANSWER: (a)

11) Which among the following is a nonlinear application of op-amp?
a. V to I converter b. Comparator
c. Precision rectifier d. Instrumentation amplifier

ANSWER: (c)

12) What is the feedback factor of voltage follower circuit?
a. Zero b. Unity
c. Infinity d. Between zero & one

ANSWER: (b)

13) For non-inverting adder, which theorem is applicable to determine the expression for output voltage?
a. Thevenin's b. Norton's
c. Miller's d. Superposition

ANSWER: (d)

14) Which among the following is/are the requirement/s of an instrumentation amplifier?
a. High slew rate b. High input resistance
c. High CMRR d. All of the above

ANSWER: (d)

15) For a temperature controller circuit comprising instrumentation amplifier, which among the following is adopted as a temperature sensor?
a. Thermistor b. Sensistor
c. Thyristor d. Thermocouple

ANSWER: (a)

16) Which parameter/s is/are used to indicate the speed of a comparator?
a. Response Time b. Propagation Delay
c. Both a and b d. None of the above

ANSWER: (c)

17) Basically, response time is defined as the time acquired by the comparator to accomplish _____ of its transition corresponding to the voltage step at the input.
a. 20% b. 50%
c. 70% d. 100%

ANSWER: (b)

18) For an ideal comparator, what should be the value of the response time?
a. Zero b. Unity
c. Infinite d. Unpredictable

ANSWER: (a)

19) Zero crossing detector circuit plays a crucial role in conversion of input sine wave into a perfect _____ at its output.
a. triangular wave b. square wave
c. saw-tooth wave d. pulse wave

ANSWER: (b)

20) For reducing the effects of input offset in comparator, what would be the possible value of input offset voltage?
a. Low b. Moderate
c. High d. None of the above

ANSWER: (a)

21) In weighted resistor DAC, how many resistor/s per bit is/are required?
a. One b. Two
c. Three d. Four

ANSWER: (a)

22) In DAC, resolution increases with the _____ in number of bits.
a. Increase b. Decrease
c. Constant d. None of the above

ANSWER: (a)

23) Which among the following characteristics of D/A converter occur/s due to resistor and semiconductor aging?
a. Speed b. Settling time
c. Long term drift d. Supply rejection

ANSWER: (c)

24) In DACs, which type of error/s specify/ies the amount by which the actual output of DAC differ from ideal straight line transfer characteristics?

a. Linearity error b. Offset error
c. Gain error d. All of the above

ANSWER: (a)

25) Offset error is basically defined as the non-zero level of analog output especially when all the digital inputs are _____.

a. 0 b. 1
c. Both a and b d. None of the above

ANSWER: (a)

26) Basically, PLL is used to lock _____

a. Its output frequency
b. Phase to the frequency
c. Phase of the input signal
d. All of the above

ANSWER: (d)

27) In communication circuits, PLL is currently applicable for _____

a. Demodulation applications
b. Tracking a carrier or synchronizing signal
c. Both a and b
d. None of the above

ANSWER: (c)

28) In the locked state of PLL, the phase error between the input & output is _____.

a. Maximum b. Moderate
c. Minimum d. All of the above

ANSWER: (c)

29) Once the phase is locked, the PLL tracks the variation in the input frequency. This indicates that _____

a. Output frequency changes by same amount as that of input frequency
b. Output frequency does not change as that of input frequency
c. There is no relation between input & output frequencies
d. None of the above

ANSWER: (a)

30) In PLL, the capture range is always _____the lock range.

a. Greater than b. Equal to
c. Less than d. None of the above

ANSWER: (c)

31) Which among the following factors affect/s the output voltage of a regulated power supply?

a. Load current b. Input voltage
c. Temperature d. All of the above

ANSWER: (d)

32) Which performance parameter of a regulator is defined as the change in regulated load voltage due to variation in line voltage in a specified range at a constant load current?

a. Load regulation b. Line regulation
c. Temperature stability factor
d. Ripple rejection

ANSWER: (b)

33) The % load regulation of a power supply should be ideally _____ & practically _____.

a. zero, small b. small, zero
c. zero, large d. large, zero

ANSWER: (a)

34) Switching regulators are series type regulators, which has _____ power dissipation & _____ efficiency.

a. increased, increased
b. increased, reduced
c. reduced, increased
d. reduced, reduced

ANSWER: (c)

35) In a linear IC voltage regulator, series pass transistor always operates in _____ region.

a. Active b. Saturation
c. Cut-off d. All of the above

ANSWER: (a)

36) Which among the following compression techniques is/ are intended for still images?

a. JPEG b. H.263
c. MPEG d. All of the above

ANSWER: (a)

37) Which lossy method for audio compression is responsible for encoding the difference between two consecutive samples?

a. Silence Compression
b. Linear Predictive Coding (LPC)
c. Adaptive Differential Pulse Code modulation (ADPCM)
d. Code Excited Linear Predictor (CELP)

ANSWER: (c)